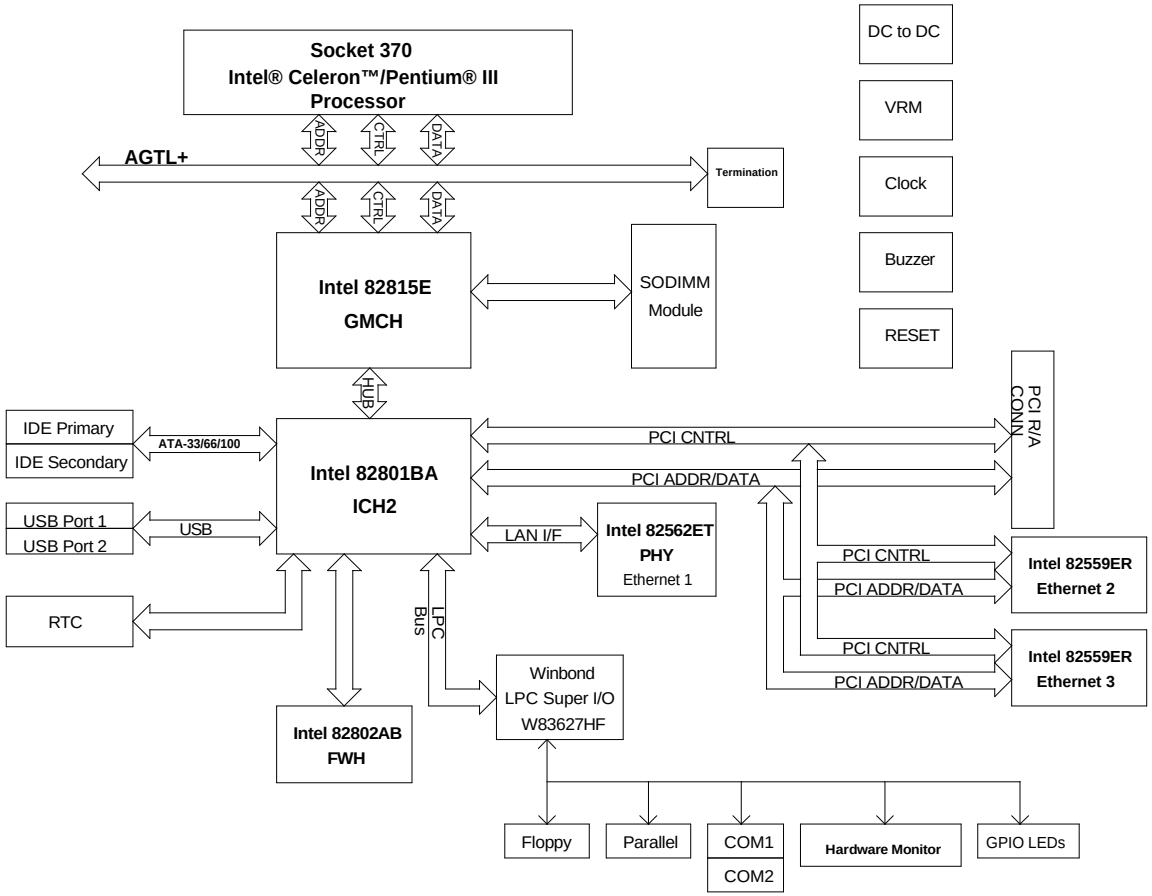
Intel® 815E Value Communications Appliance Reference Design

Block Diagram



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Note : "NP" or "-NP" means "Do not populate".
"QVL" means " Qualifed Vendor List"

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Title: BLOCK DIAGRAM		
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General Board Design Requirements

>> PCB must be routed using six (6) layers, with the following stackup:

Layer 1: Signal, V2P5,V1P8
Layer 2: GND
Layer 3: Signal
Layer 4: Signal
Layer 5: Split Power Plane --V5P0 and V3P3 Plane,
Vcore Island
Layer 6: Signal, V1P5

>> Right angle traces must not be used.

>> Vias for decoupling capacitors must be kept as close as possible to the capacitor pad.

>> Trace impedance must be 60 ohms, +/- 15%

>> Total board thickness must be .062".

>> Board material must be FR-4.

>> GND layers must not be split.

>> Top and bottom (outer) layers must be no less than 1/2 oz copper before plating, inner layers must be 1 oz copper.

>> Series terminating resistors must be kept as close to the driving pin as possible.

>> Daisy chain signals going to more that on point, do not use stubs.

>> Unless otherwise noted, all signal traces must be between 5 and 6 mil width.

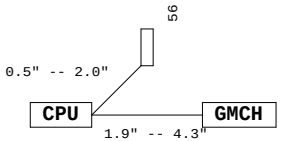
>> Unless otherwise noted, minimum space between traces is 10 mils, including adjacent layers.

>> Specific routing reqirements are included throughout schematic sheets.

>> One registration target must be included on each corner of the board.

CPU Routing Requirements

>> Route all GTL traces between CPU and GMCH as shown in the diagram to the right.



>> Route all traces between CPU and GMCH on a layer adjacent to a ground plane, without layer changes.

>> Minimum space between traces is 10 mils (unless otherwise noted), this includes adjacent signal layers.

>> Minimum space between traces may be reduced to 5 mils when breaking out of a footprint. The total length of trace routed using 5 mil spacing must be less than 250 mils.

>> The following signals require 25 mil spacing from other traces, including adjacent layers.

HA#[31:3], HD#[63:0], BREQ#0, HADS#, BNR#, BPRI#, HLOCK#, DEFER#, HTRDY#, DBSY#, DRDY#, HIT#, HITM#, A20M#, IGNNE#, INIT#, INTR, NMI, PWR_OK_2P5, SMI#, CPUSLP#, STPCLK#, 66#/100SEL,100#/133SEL,FERR#,CPURST#, HREQ#[4:0], RS#[2:0], GTLREF[7:0], PLL[2:1], (CPU_TCK/TMS/TDI/TDO/TRST#, PRDY#, PREQ#).

>> AGTL+ signals must be well isolated from system memory sgnals. AGTL+ signal trace edges must be at least 30 mils from system memory trace edges within 100 mils of the ball of the GMCH.

>> Route GTLREF using 25 mil minimum width trace, and separate from all other traces by 25 mils minimum.

>> Route PLL[2:1] using 25 mil minimum width trace, minimize loop area, and separate from all other traces by 25 mils minimum.

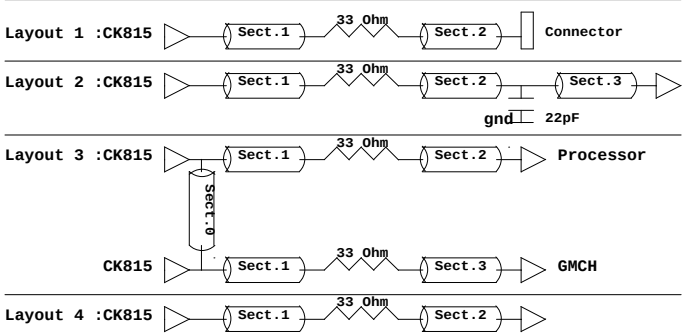
Clock Specific Routing Requirements

>> A clock trace must not alternate layers.

>> All clocks should be routed 5 mils with 15 mils spacing to any other signals.

>> Serial resisters : 22 ohm for MEMCLK0,1,DCLK_WR and 33 ohm for the others.

Topologies



Routing Solution : **Note : A < 6"**

Destination	Topologies	Sect.0	Sect.1	Sect.2	Sect.3
MEMCLK0,1	Layout1	N/A	<0.5"	A	N/A
DCLK_WR	Layout2	N/A	<0.5"	A+3.5"	0.5"
CPUHCLK	Layout3	<0.1"	<0.5"	A+5.2"	N/A
GMCHHCLK	Layout3	<0.1"	<0.5"	N/A	A+8"
GMCH_3V66	Layout4	N/A	<0.5"	A+8"	N/A
ICH_3V66	Layout4	N/A	<0.5"	A+8"	N/A
PCLKICH	Layout4	N/A	<0.5"	A+8"	N/A
PCLK559A,B; PCLKFWH ; PCLKSIO	Layout4	N/A	<0.5"	A+8.5" to A+14"	N/A
PCICLKA	Layout4	N/A	<0.5"	A+5" to A+11"	N/A

Power Supply Specific Routing Requirements

>> All unrelated signals and power planes must be kept away from the switching circuits.

>> All traces associated with the input power/ground connectors, and the capacitors connected to these connectors, must be routed with minimum length and maximum width.

>> See the Power Supply schematic sheet for complete restrictions.

Memory Bus Specific Routing Requirements

>> Minimum trace width is 5 mils.

>> Minimum space between traces is 10 mils, this includes adjacent signal layers.

>> Minimum space between memory traces and other types of traces is 25 mils, this includes adjacent signal layers.

>> Memory address, data, and control lines must be routed as separate groups and treated as different signal types.

>> The SM_MD,SM_DQMA,SM_CSA#,SM_RAS#,SM_CAS#, SM_WE#, and SM_MA signals (between GMCH and SODIMM) must be between 1" and 3.5" in length, matched to within 600 mils.

Memory Bus GROUPS -- SO-DIMM Names

>> Address Signals : SM_MAA[13:0]

>> Data signals : SM_MD[63:0]

>> Control Signals:

SMBDATA, SMBCLK, SM_CSA[1:0]#, SM_WE#, SM_CAS#,SM_RAS#

PCI Bus Specific Routing Requirements

>> PCI bus max length must be less than 6".

PCI Bus GROUPS

>> Address/Data Signals: AD[31:0]

>> Control Signals:

C/BE[3:0]#, REQ[4:1]#, GNT[4:1]#, INT[A:D]#, PCIRST#, FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, SERR#, PERR#, PAR, LOCK#

HUB Bus GROUPS

>> Address/Data Signals: HL[10:0]

>> Control Signals: HLSTB,HLSTB# (differential strobe pair).

>> HL[10:0] should be routed with a trace width of 5 mils and a trace spacing of 20 mils. These signals can be routed with a trace width of 5 mils and a trace spacing of 15 mils for navigation around components or mounting holes. The maximum trace length for the hub interface data signals is 7". These signals should each be matched within .1"" of the HLSTB and HLSTB# signals.

IDE Specific Routing Requirements

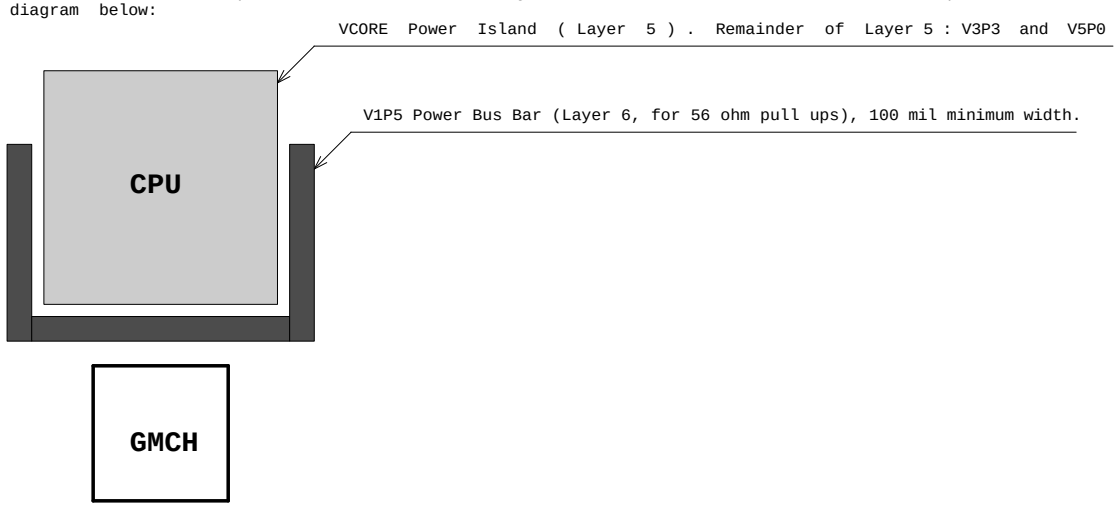
>> Place IDE conector within 8" of ICH.

>> IDE interface : 5 mils trace , spaces >= 5 mils

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CPU/GMCH Specific Routing Requirements.

>> Rotate the CPU and GMCH chips so as to minimize the length of the connections between the two, and place as shown in the diagram below:



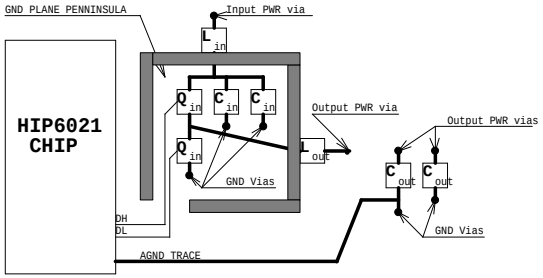
>> The VCORE power supply must not be layed over the VCORE power island. The power supply feed to the power island must be the maximum practical width.

>> The V1P5 power supply must not be layed over the V1P5 power island. The power supply feed to the power island must be the maximum practical width.

>> The VCORE power island depiction above, is approximate, and must be large enough to fully encompass the entire CPU as well as any component that connects to the VCORE supply.

Power Supply specific Routing Requirements.

>> The diagram below depicts the placement requirements for the HIP6021 switching regulator circuits. A GND plane penninsula is used to contain the high current and noisy switching components. All of the bold traces and vias shown have high current and low impedance requirements. These trace widths should be 100 mils minimum. The channel which connects the GND penninsula to the main GND plane must be 500 mils in width.

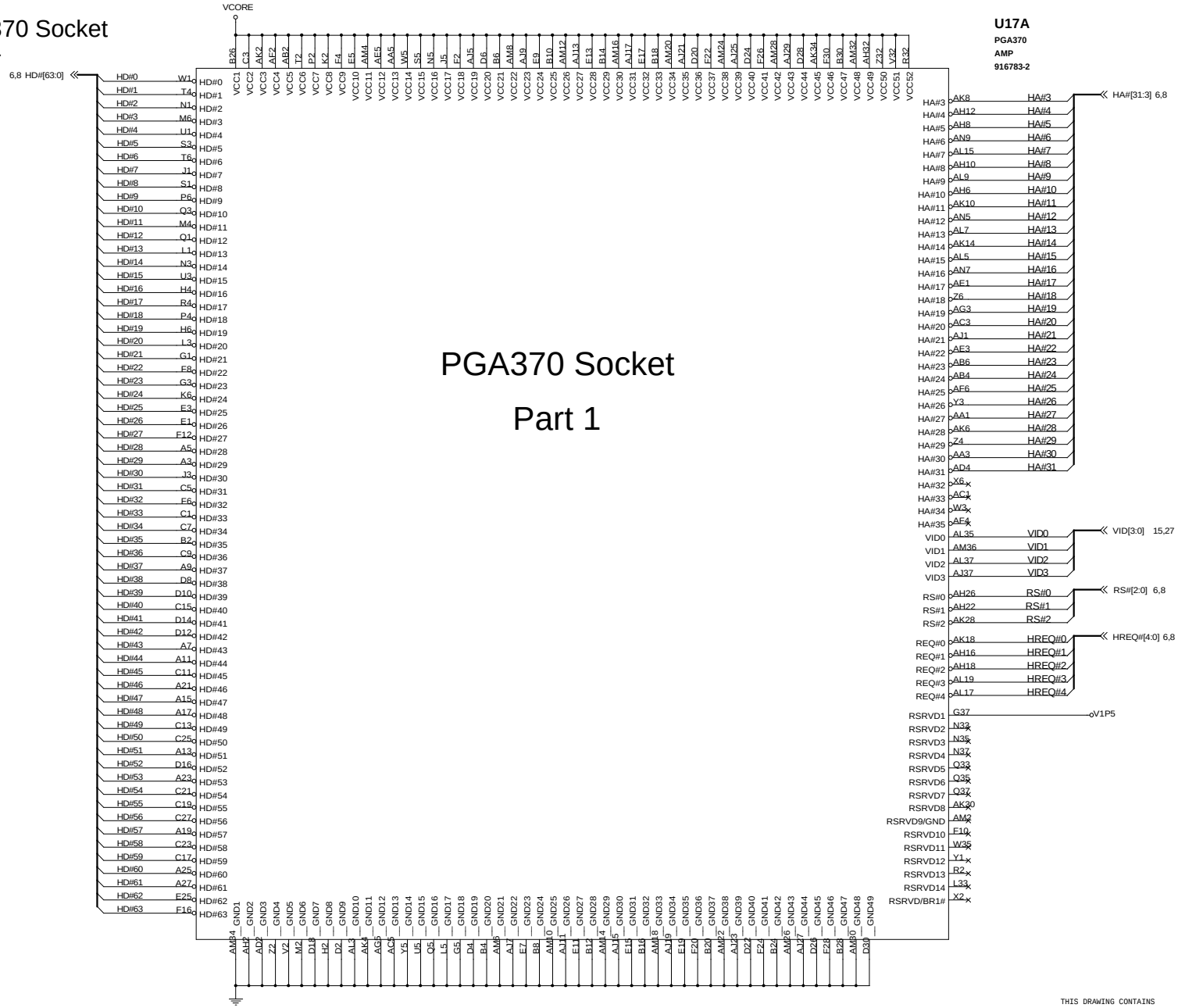


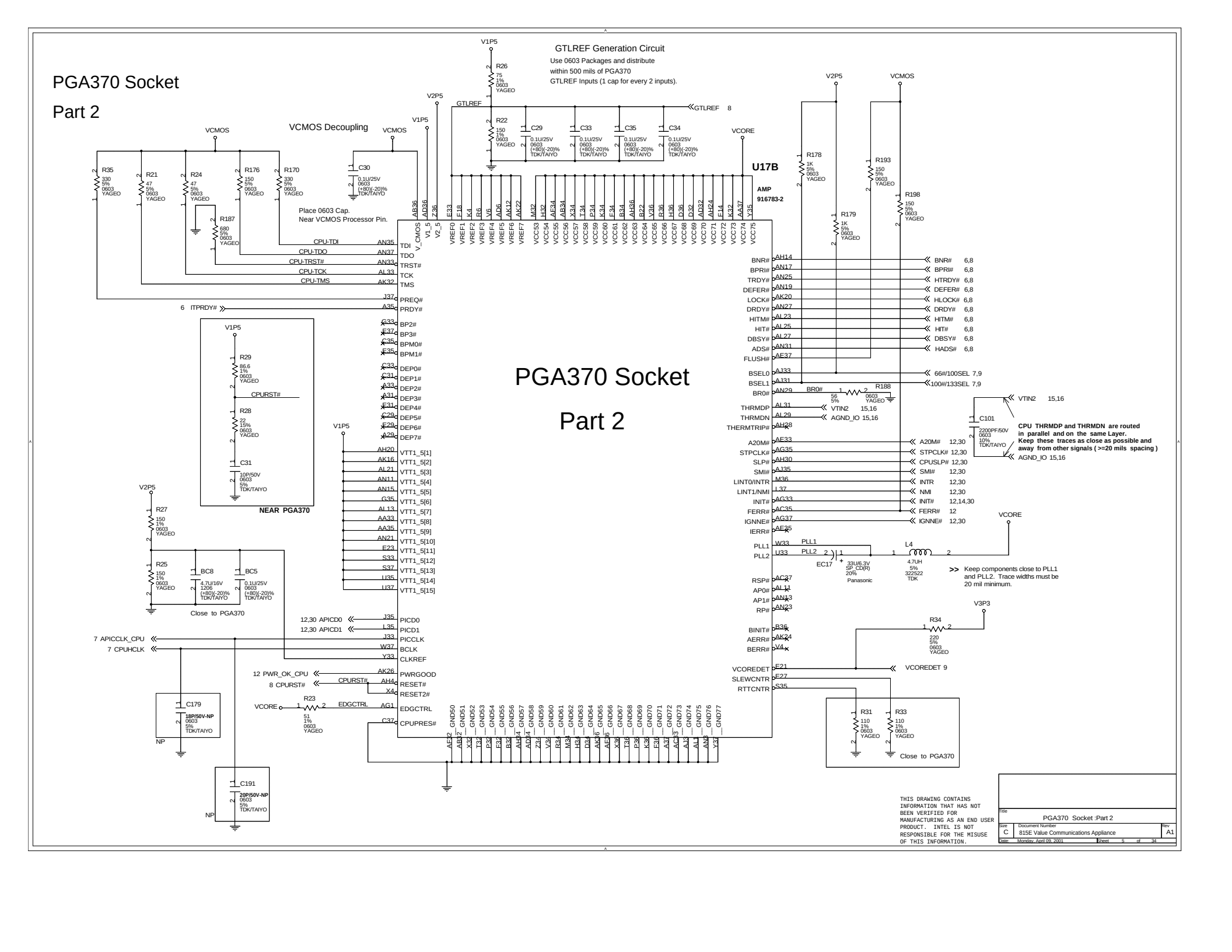
>> No other signals may be routed underneath the GND plane penninsula.

>> No other power planes may exist underneath the GND plane penninsula.

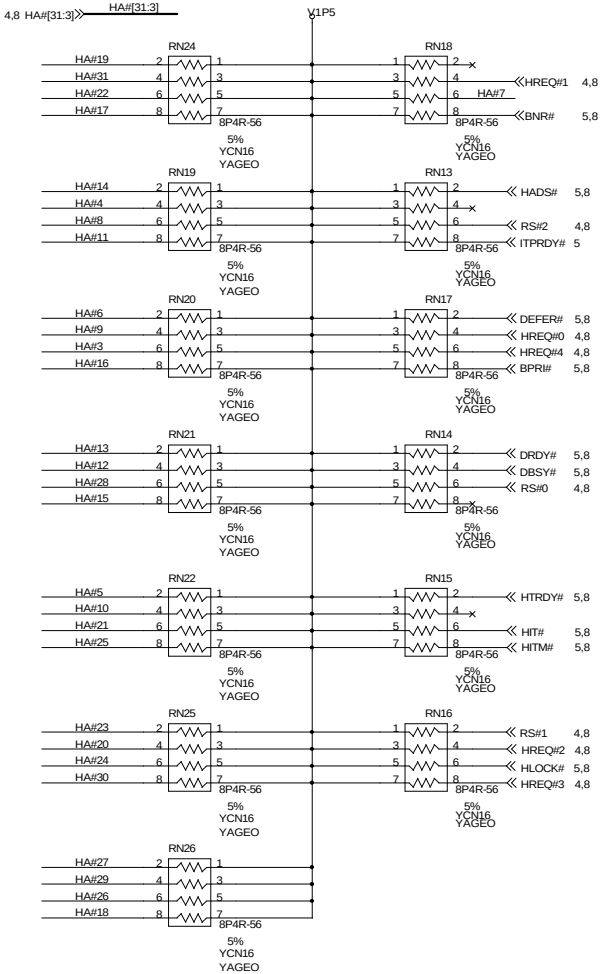
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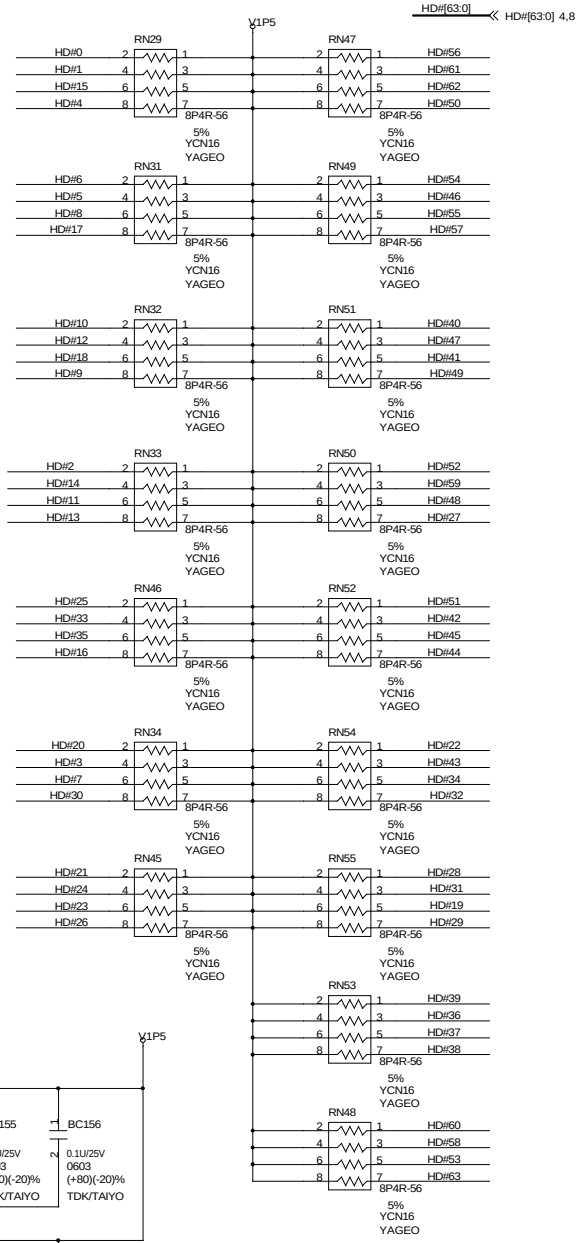
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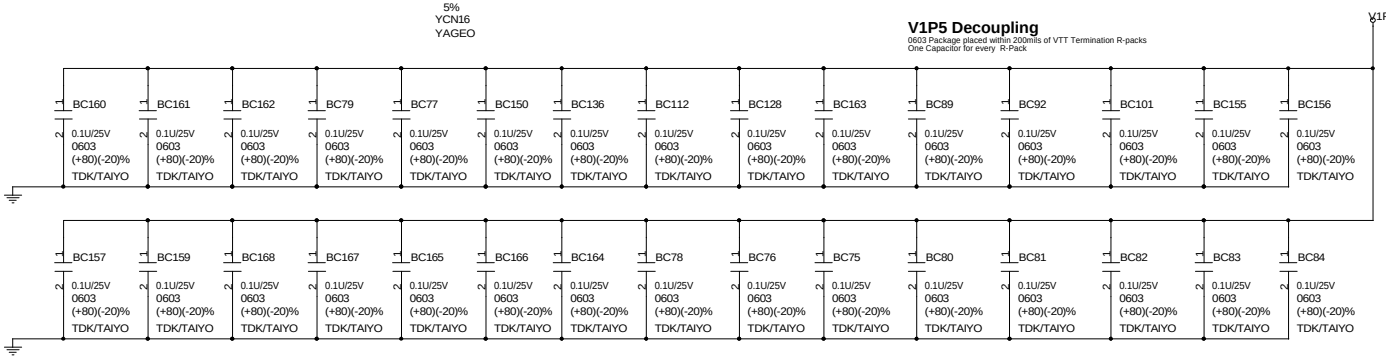

PGA370 Socket
Part 1
VCORE
U17A
PGA370
AMP
916783-2
6,8 HD#[63:0]
HD#0 W1
HD#1 T4
HD#2 N1
HD#3 M6
HD#4 U1
HD#5 S3
HD#6 T6
HD#7 J1
HD#8 S1
HD#9 P6
HD#10 Q3
HD#11 M4
HD#12 Q1
HD#13 L1
HD#14 N3
HD#15 U3
HD#16 H4
HD#17 R4
HD#18 P4
HD#19 H6
HD#20 L3
HD#21 G1
HD#22 F8
HD#23 G3
HD#24 K6
HD#25 E3
HD#26 E1
HD#27 F12
HD#28 A5
HD#29 A3
HD#30 J3
HD#31 C5
HD#32 E6
HD#33 C1
HD#34 C7
HD#35 B2
HD#36 C9
HD#37 A9
HD#38 D8
HD#39 D10
HD#40 C15
HD#41 D14
HD#42 D12
HD#43 A7
HD#44 A11
HD#45 C11
HD#46 A21
HD#47 A15
HD#48 A17
HD#49 C13
HD#50 C25
HD#51 A13
HD#52 D16
HD#53 A23
HD#54 C21
HD#55 C19
HD#56 C27
HD#57 A19
HD#58 C23
HD#59 C17
HD#60 A25
HD#61 A27
HD#62 E25
HD#63 F16
HA#3 AK8
HA#4 AH12
HA#5 AH8
HA#6 AN9
HA#7 AL15
HA#8 AH10
HA#9 AL9
HA#10 AH6
HA#11 AK10
HA#12 AN5
HA#13 AL7
HA#14 AK14
HA#15 AL5
HA#16 AN7
HA#17 AE1
HA#18 Z6
HA#19 AG3
HA#20 AC3
HA#21 AJ1
HA#22 AE3
HA#23 AB6
HA#24 AB4
HA#25 AF6
HA#26 Y3
HA#27 AA1
HA#28 AK6
HA#29 Z4
HA#30 AA3
HA#31 AD4
HA#32 X6
HA#33 AC1
HA#34 W3
HA#35 AF4
HA#[31:3] 6,8
VID0 AL35
VID1 AM36
VID2 AL37
VID3 AJ37
VID[3:0] 15,27
RS#0 AH26
RS#1 AH22
RS#2 AK28
RS#[2:0] 6,8
REQ#0 AK18
REQ#1 AH16
REQ#2 AH18
REQ#3 AL19
REQ#4 AL17
HREQ#[4:0] 6,8
RSRVD1 G37
RSRVD2 N33
RSRVD3 N35
RSRVD4 N37
RSRVD5 Q33
RSRVD6 Q35
RSRVD7 Q37
RSRVD8 AK30
RSRVD9/GND AM2
RSRVD10 F10
RSRVD11 W35
RSRVD12 Y1
RSRVD13 R2
RSRVD14 L33
RSRVD/BR1# X2
V1P5
PGA370 Socket
Part 1
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PGA370 Socket
Part 2
GTLREF Generation Circuit
Use 0603 Packages and distribute
within 500 mils of PGA370
GTLREF Inputs (1 cap for every 2 inputs).
VCMOS Decoupling
Place 0603 Cap.
Near VCMOS Processor Pin.
U17B
AMP
916783-2
PGA370 Socket
Part 2
NEAR PGA370
Close to PGA370
Close to PGA370
CPU THRMDP and THRMDN are routed
in parallel and on the same Layer.
Keep these traces as close as possible and
away from other signals (>=20 mils spacing)
>> Keep components close to PLL1
and PLL2. Trace widths must be
20 mil minimum.
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PGA370 Socket :Part 2
815E Value Communications Appliance
Monday, April 09, 2001

AGTL+ Termination







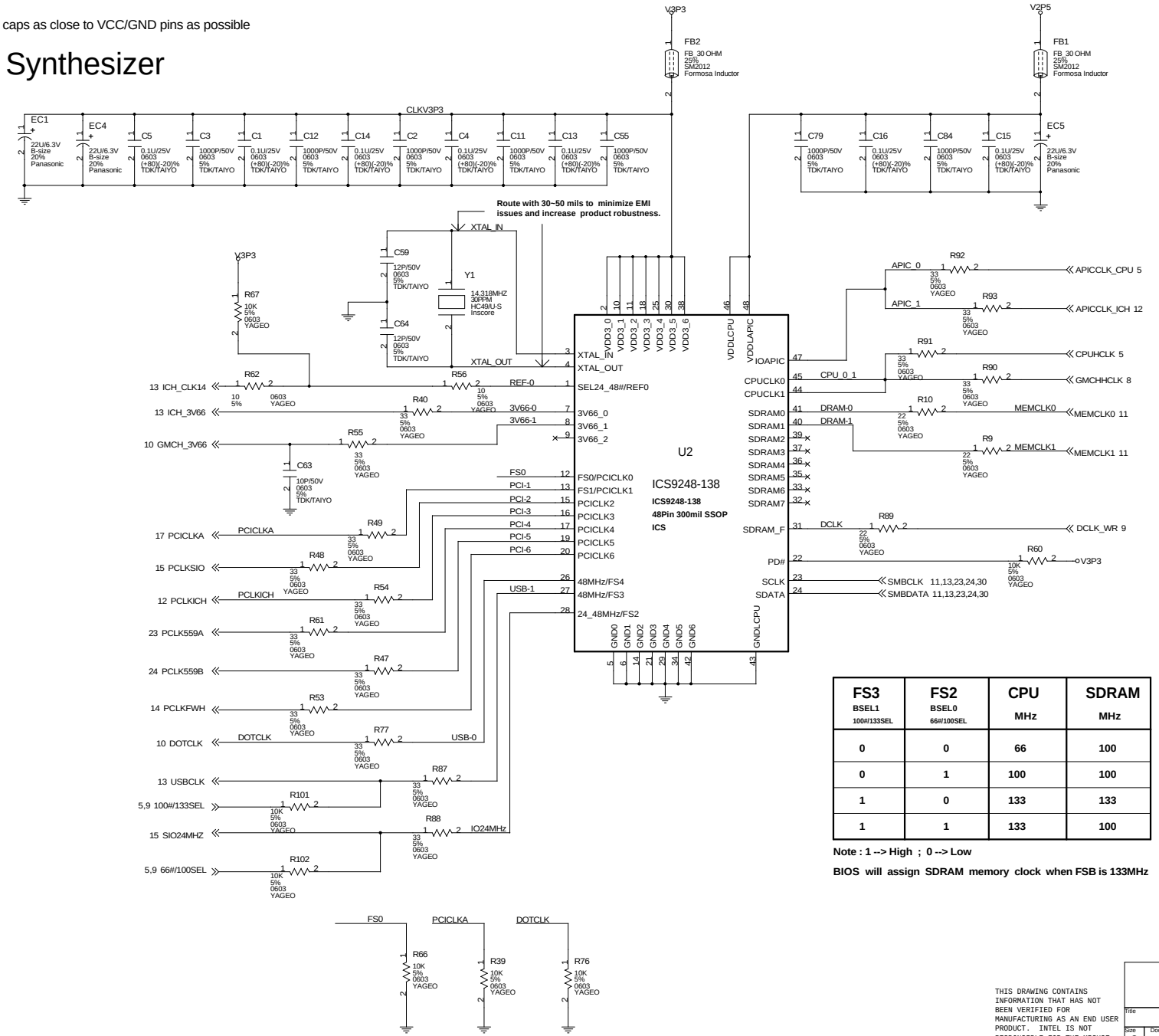
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Notes:

- Place all decoupling caps as close to VCC/GND pins as possible

Clock Synthesizer



FS3 BSEL1 100#/133SEL	FS2 BSEL0 66#/100SEL	CPU MHz	SDRAM MHz
0	0	66	100
0	1	100	100
1	0	133	133
1	1	133	100

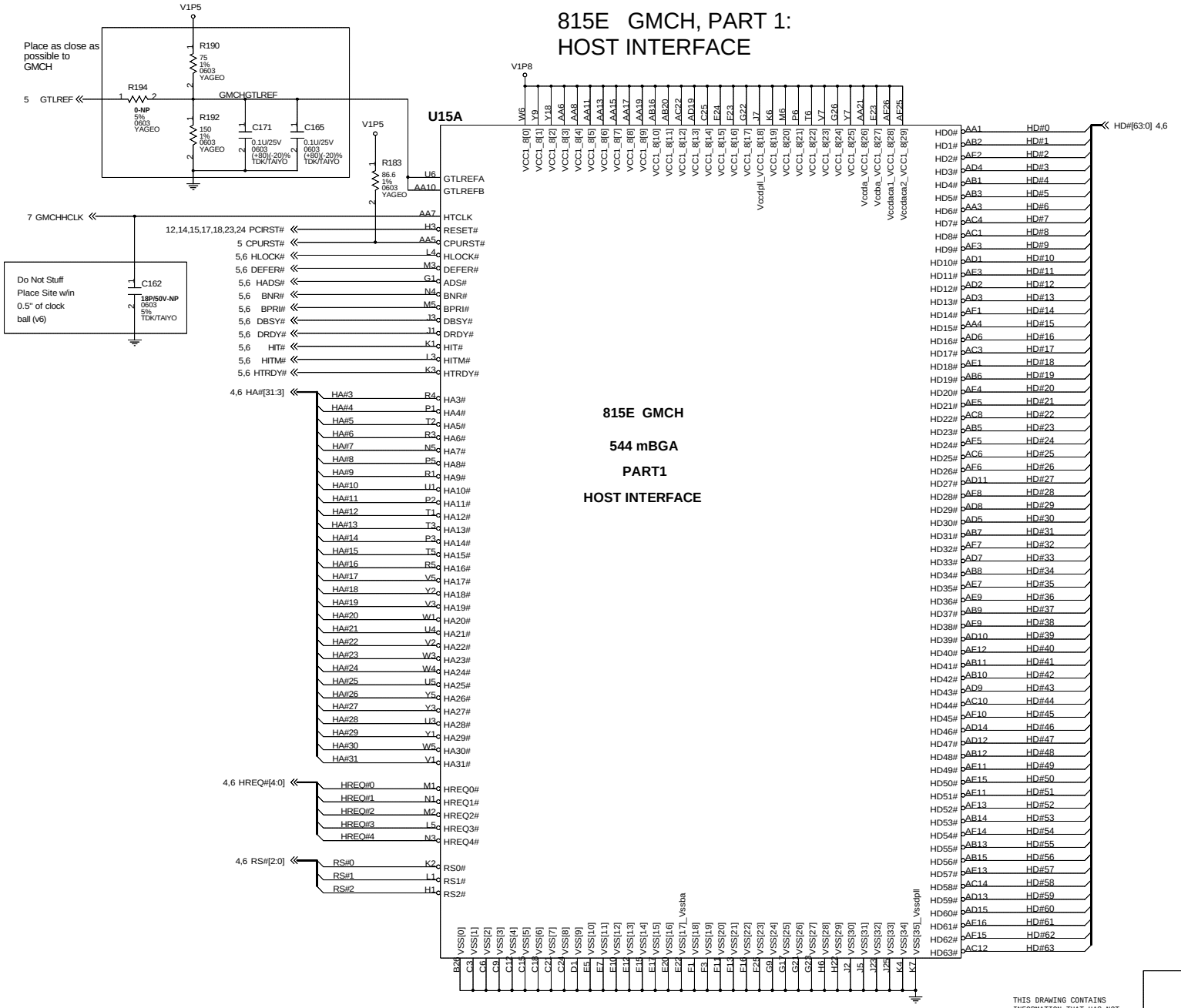
Note : 1 --> High ; 0 --> Low

BIOS will assign SDRAM memory clock when FSB is 133MHz

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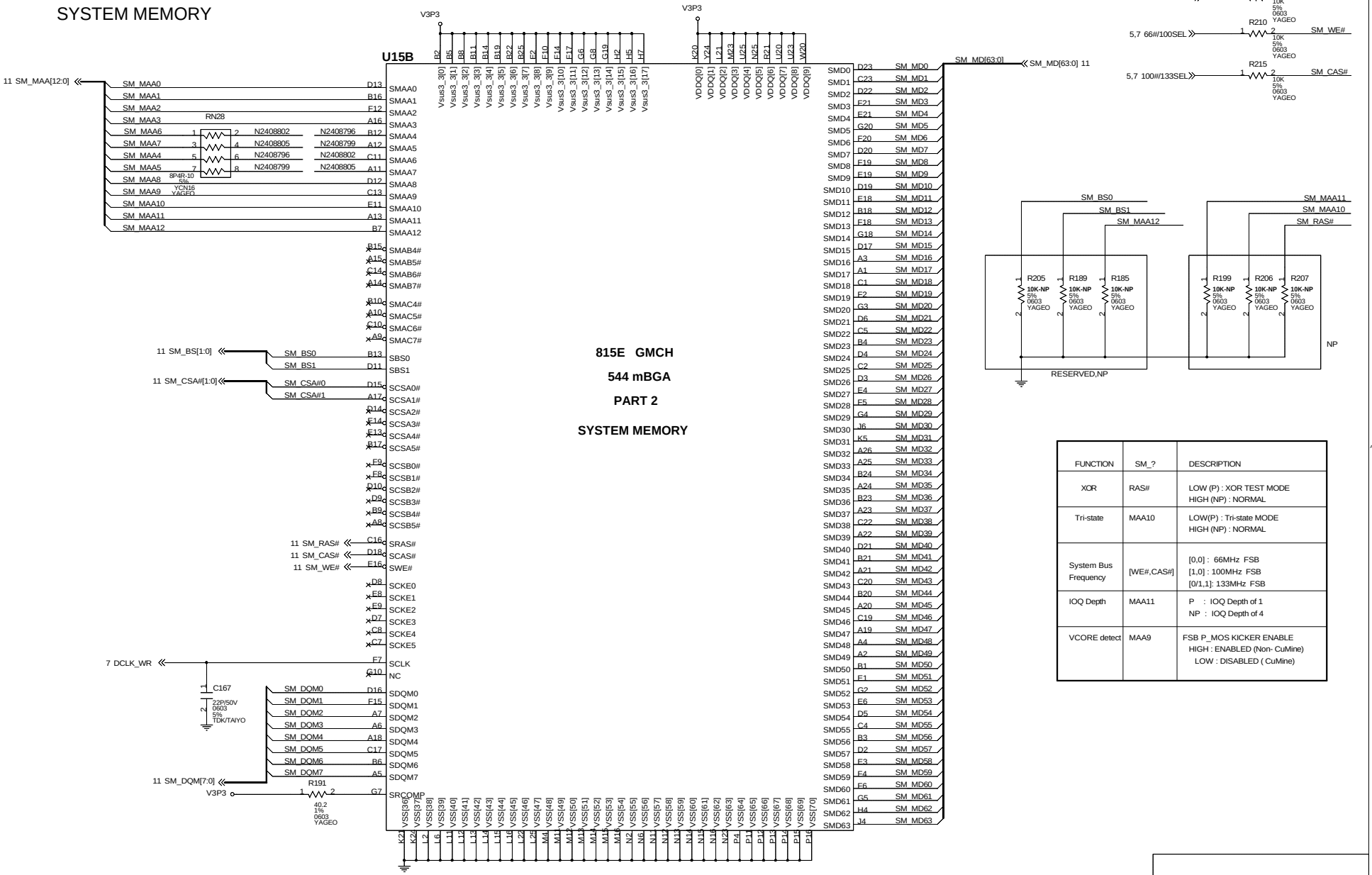
Title	CLOCK Synthesizer	
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815E GMCH, PART 1: HOST INTERFACE



815E GMCH, PART 2:

SYSTEM MEMORY

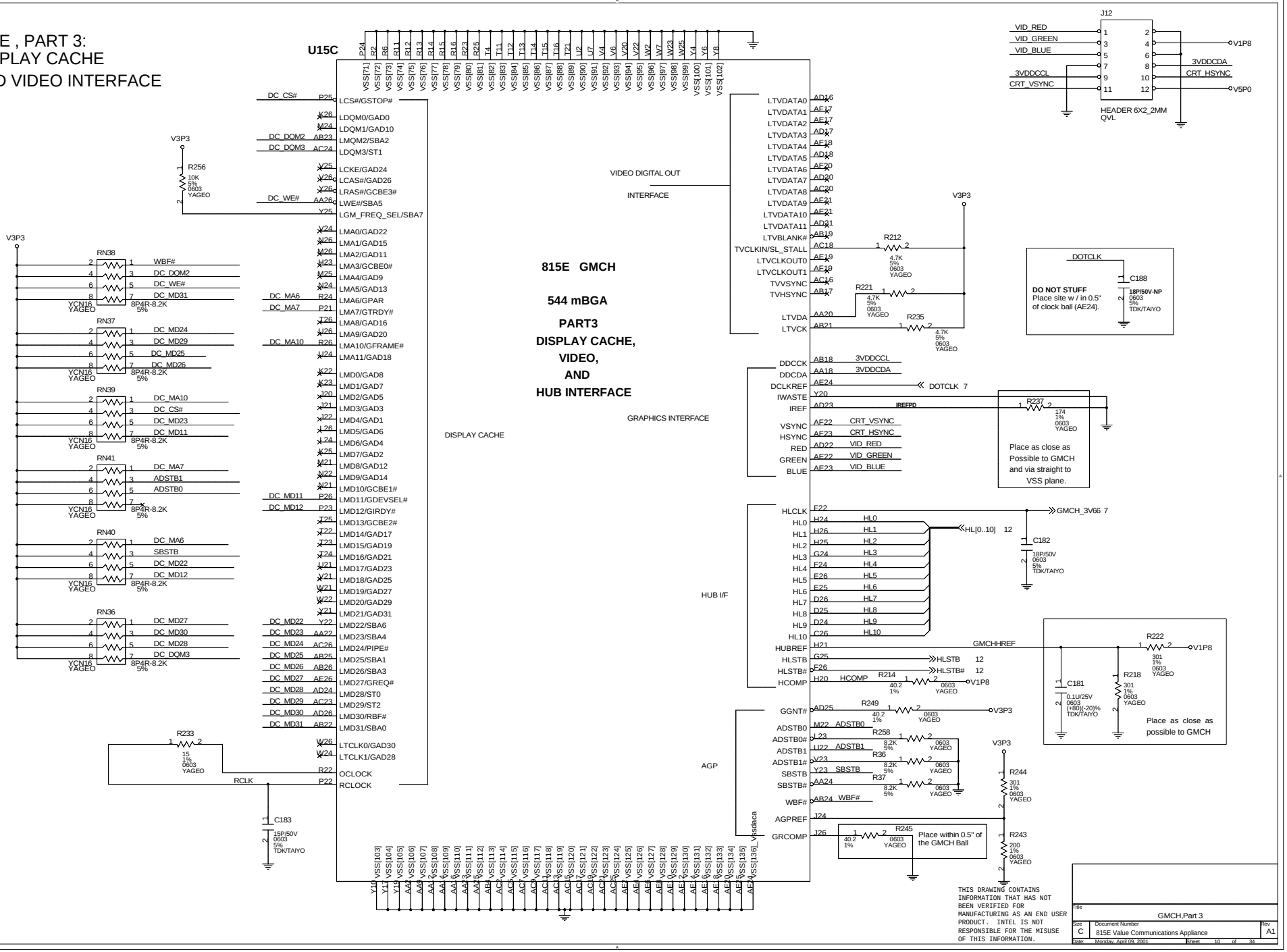


FUNCTION	SM_?	DESCRIPTION
XOR	RAS#	LOW (P) : XOR TEST MODE HIGH (NP) : NORMAL
Tri-state	MAA10	LOW(P) : Tri-state MODE HIGH (NP) : NORMAL
System Bus Frequency	[WE#,CAS#]	[0,0] : 66MHz FSB [1,0] : 100MHz FSB [0/1,1]: 133MHz FSB
IOQ Depth	MAA11	P : IOQ Depth of 1 NP : IOQ Depth of 4
VCORE detect	MAA9	FSB P_MOS KICKER ENABLE HIGH : ENABLED (Non- CuMine) LOW : DISABLED (CuMine)

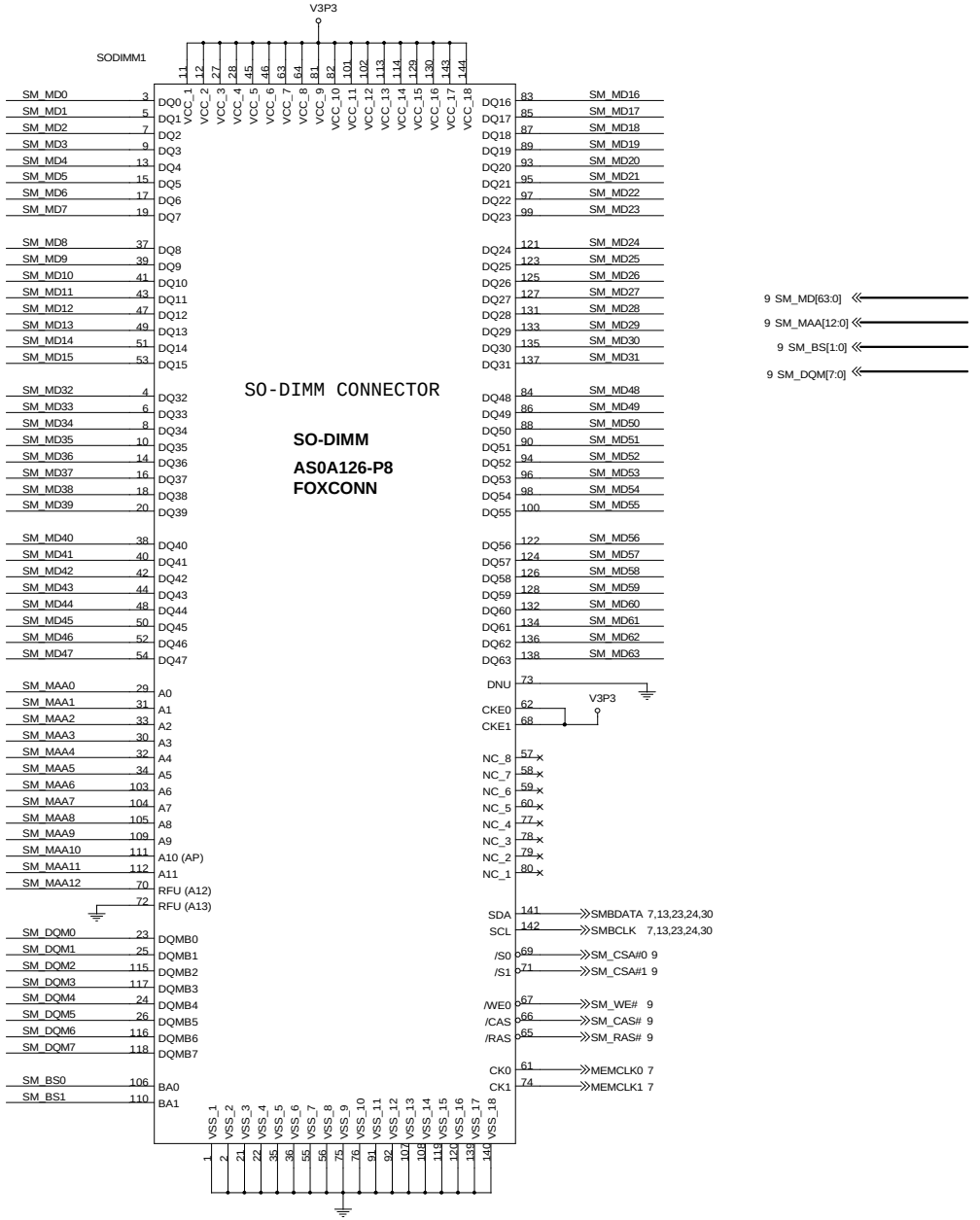
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815E , PART 3:
DISPLAY CACHE
AND VIDEO INTERFACE

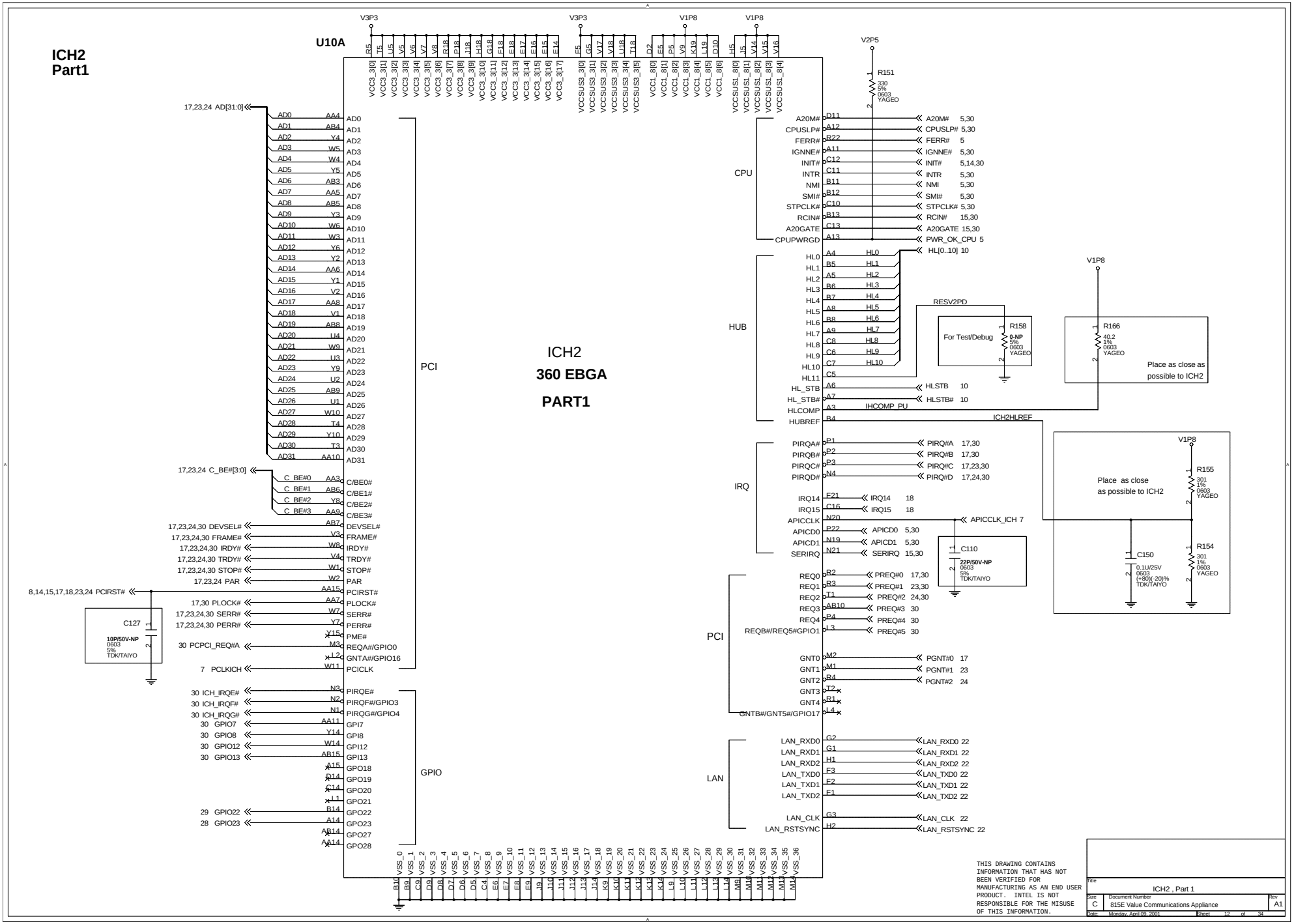


SYSTEM MEMORY

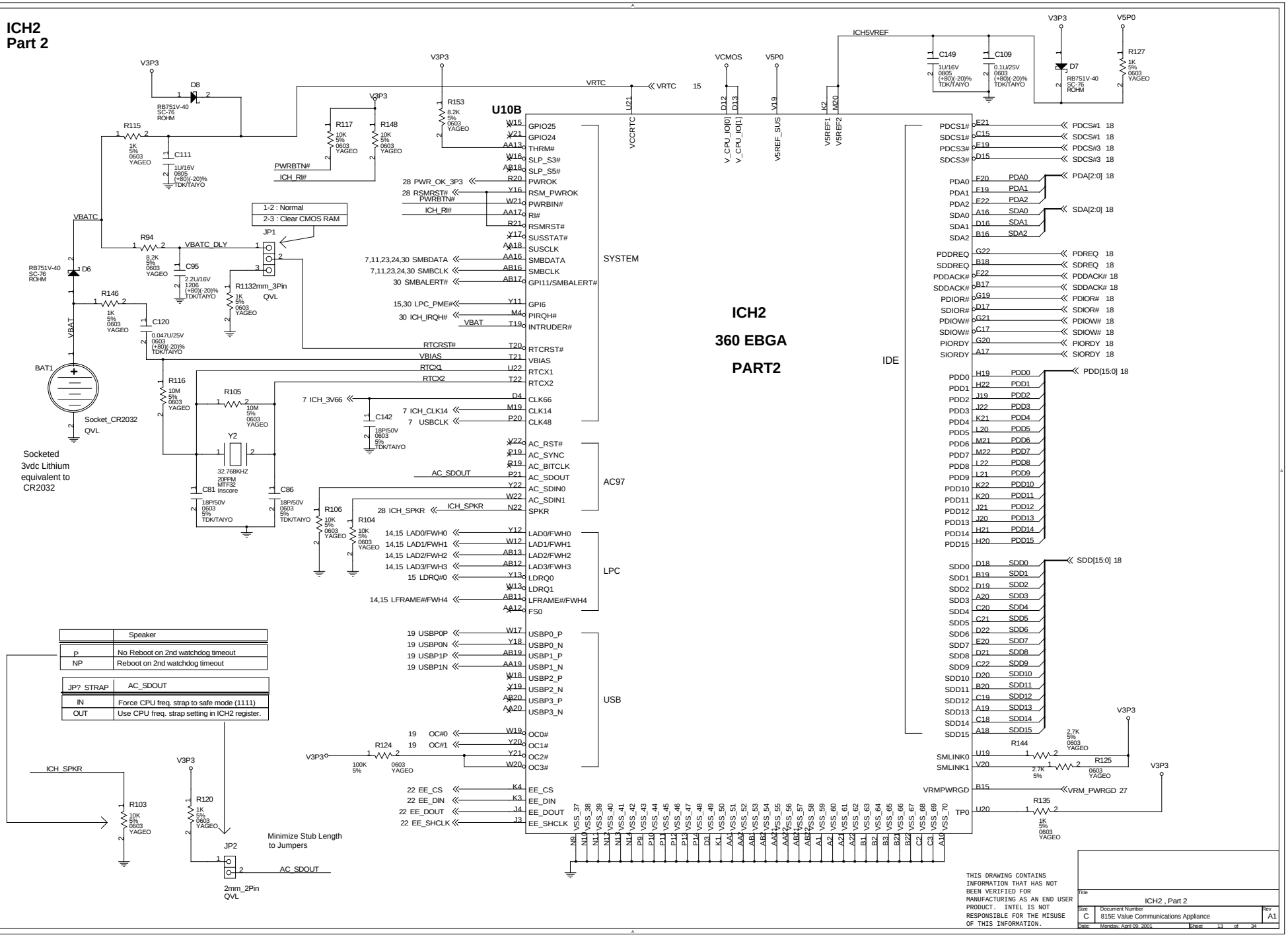


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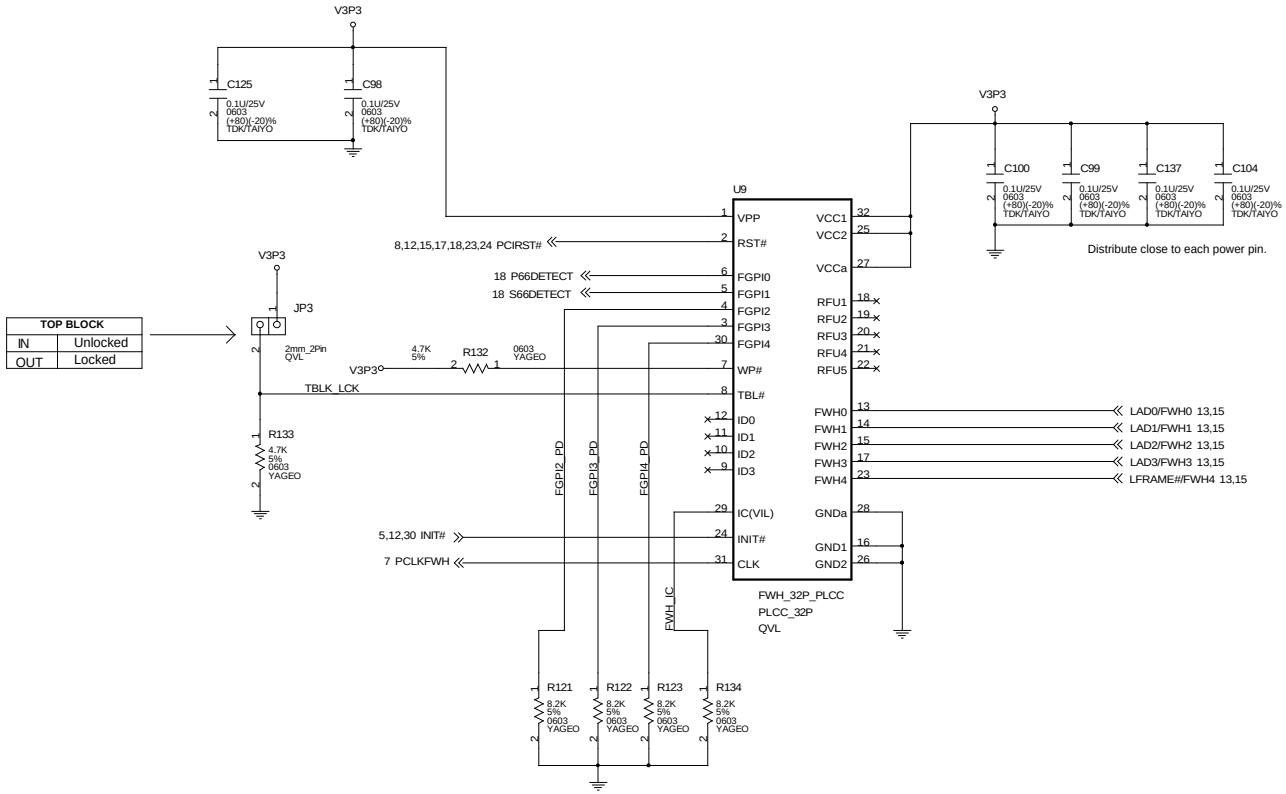

ICH2
Part1
U10A
ICH2
360 EBGA
PART1
PCI
GPIO
CPU
HUB
IRQ
PCI
LAN
V3P3
V1P8
V2P5
R151
330
5%
0603
YAGEO
RESV2PD
For Test/Debug
R158
0-NP
5%
0603
YAGEO
R166
40.2
1%
0603
YAGEO
Place as close as possible to ICH2
IHCOMP_PU
ICH2HLREF
Place as close as possible to ICH2
R155
301
1%
0603
YAGEO
R154
301
1%
0603
YAGEO
C150
0.1U/25V
0603
(+80)(-20)%
TDK/TAIYO
C110
22P/50V-NP
0603
5%
TDK/TAIYO
C127
10P/50V-NP
0603
5%
TDK/TAIYO
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ICH2
Part 2


U10B
ICH2
360 EBGA
PART2
SYSTEM
AC97
LPC
USB
IDE
GPIO25
GPIO24
THRM#
SLP_S3#
SLP_S5#
PWROK
RSM_PWROK
PWRBIN#
RI#
RSMRST#
SUSSTAT#
SUSCLK
SMBDATA
SMBCLK
GPI11/SMBALERT#
GPI6
PIRQH#
INTRUDER#
RTCRST#
VBIAS
RTCX1
RTCX2
CLK66
CLK14
CLK48
AC_RST#
AC_SYNC
AC_BITCLK
AC_SDOUT
AC_SDIN0
AC_SDIN1
SPKR
LAD0/FWH0
LAD1/FWH1
LAD2/FWH2
LAD3/FWH3
LDRQ0
LDRQ1
LFRAME#/FWH4
FS0
USBP0_P
USBP0_N
USBP1_P
USBP1_N
USBP2_P
USBP2_N
USBP3_P
USBP3_N
OC0#
OC1#
OC2#
OC3#
EE_CS
EE_DIN
EE_DOUT
EE_SHCLK
V_CPU_IO[0]
V_CPU_IO[1]
V5REF_SUS
V5REF1
V5REF2
VCCRTC
PDCS1#
SDCS1#
PDCS3#
SDCS3#
PDA0
PDA1
PDA2
SDA0
SDA1
SDA2
PDDREQ
SDDREQ
PDDACK#
SDDACK#
PDIOR#
SDIOR#
PDIOW#
SDIOW#
PIORDY
SIORDY
PDD0
PDD1
PDD2
PDD3
PDD4
PDD5
PDD6
PDD7
PDD8
PDD9
PDD10
PDD11
PDD12
PDD13
PDD14
PDD15
SDD0
SDD1
SDD2
SDD3
SDD4
SDD5
SDD6
SDD7
SDD8
SDD9
SDD10
SDD11
SDD12
SDD13
SDD14
SDD15
SMLINK0
SMLINK1
VRMPWRGD
TP0
VSS_37
VSS_38
VSS_39
VSS_40
VSS_41
VSS_42
VSS_43
VSS_44
VSS_45
VSS_46
VSS_47
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VSS_64
VSS_65
VSS_66
VSS_67
VSS_68
VSS_69
VSS_70
V3P3
V5P0
VCMOS
VRTC
ICH5VREF
PWRBTN#
ICH_R#
PWR_OK_3P3
RSMRST#
VBATC
VBAT
VBATC_DLY
VBIAS
RTCX1
RTCX2
AC_SDOUT
ICH_SPKR
LFRAME#/FWH4
LDRQ#0
SMBDATA
SMBCLK
SMBALERT#
LPC_PME#
ICH_IRQH#
PDCS#1
PDCS#3
PDA[2:0]
SDA[2:0]
PDDREQ
SDDREQ
PDDACK#
SDDACK#
PDIOR#
SDIOR#
PDIOW#
SDIOW#
PIORDY
SIORDY
PDD[15:0]
SDD[15:0]
VRM_PWRGD
D8
D6
D7
BAT1
Socket_CR2032
QVL
Socketed
3vdc Lithium
equivalent to
CR2032
Y2
32.768KHZ
20PPM
MTF32
JP1
1-2 : Normal
2-3 : Clear CMOS RAM
R1132mm_3Pin
JP2
2mm_2Pin
Minimize Stub Length
to Jumpers
Speaker
P
No Reboot on 2nd watchdog timeout
NP
Reboot on 2nd watchdog timeout
JP? STRAP
AC_SDOUT
IN
Force CPU freq. strap to safe mode (1111)
OUT
Use CPU freq. strap setting in ICH2 register.
THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.
Title
ICH2 , Part 2
Size
C
Document Number
815E Value Communications Appliance
Rev
A1
Date:
Monday, April 09, 2001
Sheet
13
of
34

FirmWare Hub (FWH) Socket

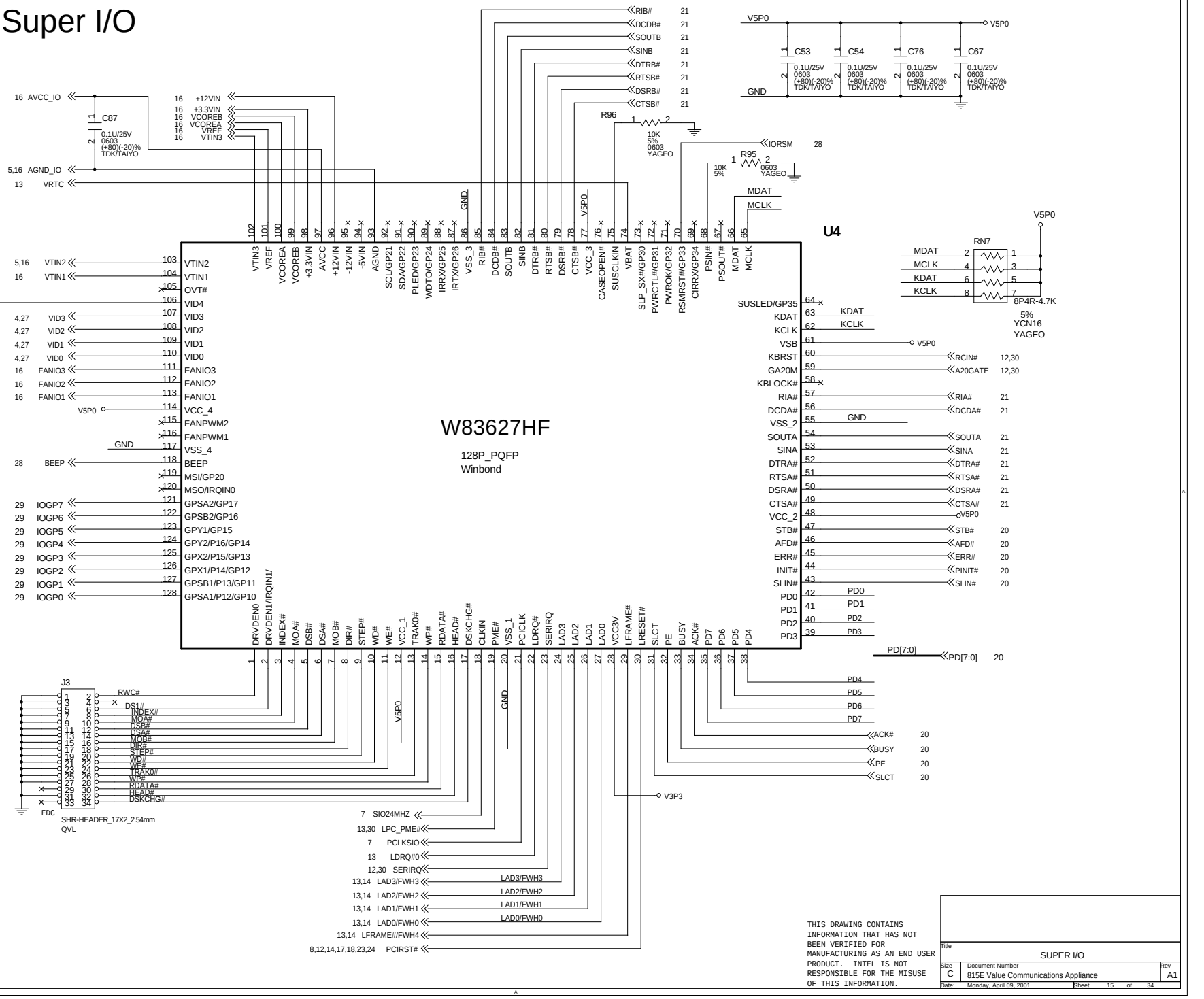
NOTE: This is a Socketed Implementation



THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

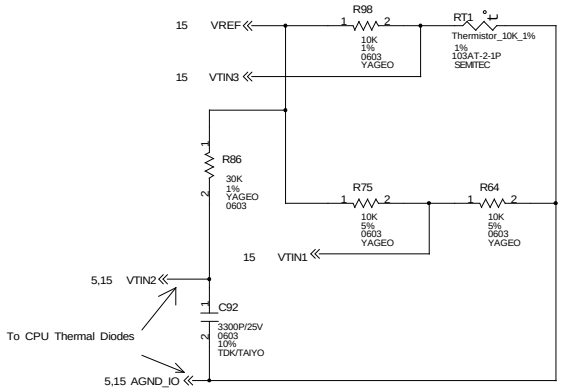
Title	FIRMWARE HUB (FWH)	
Size: C	Document Number: 815E Value Communications Appliance	Rev: A1
Date: Monday, April 09, 2001	Sheet 14 of 34	

Super I/O

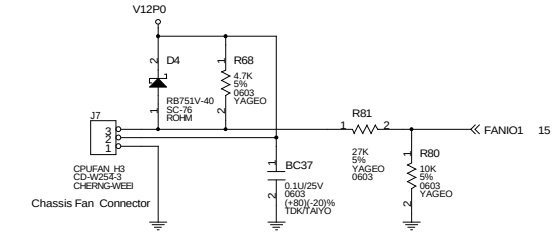

W83627HF
128P_PQFP
Winbond
U4
J3
SHR-HEADER_17X2_2.54mm
QVL
FDC
8P4R-4.7K
5%
YCN16
YAGEO
THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.
SUPER I/O
815E Value Communications Appliance
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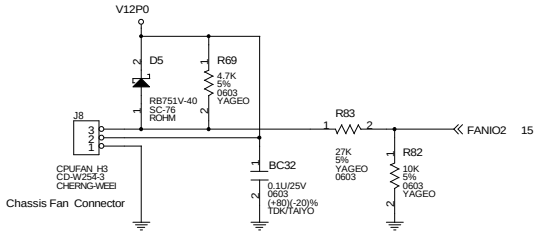
Hardware Monitor circuits

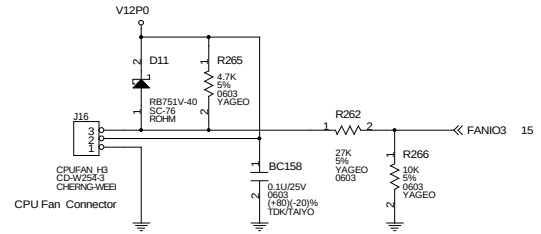
Temperature Sensing



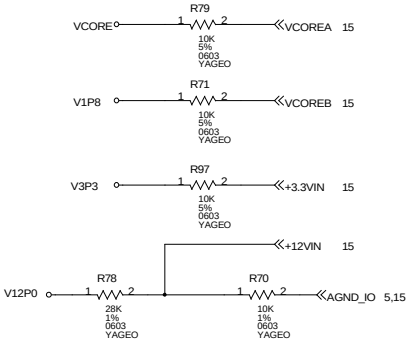
RT1: Sense System Temperature

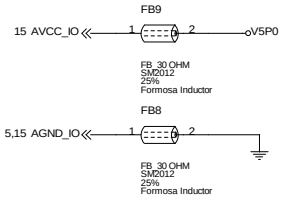






Voltage Sensing

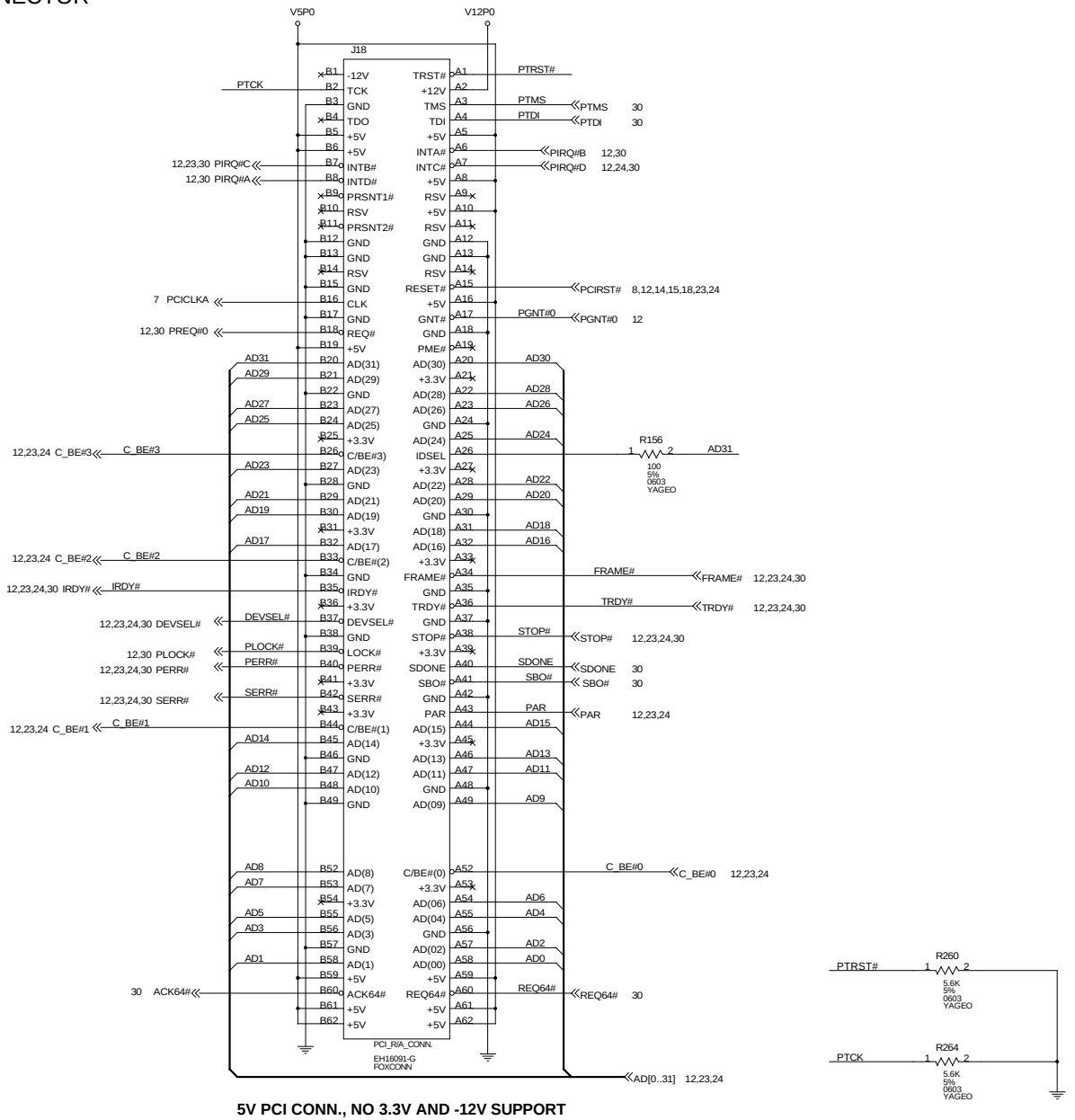




THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title	Hardware Monitor	
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PCI CONNECTOR

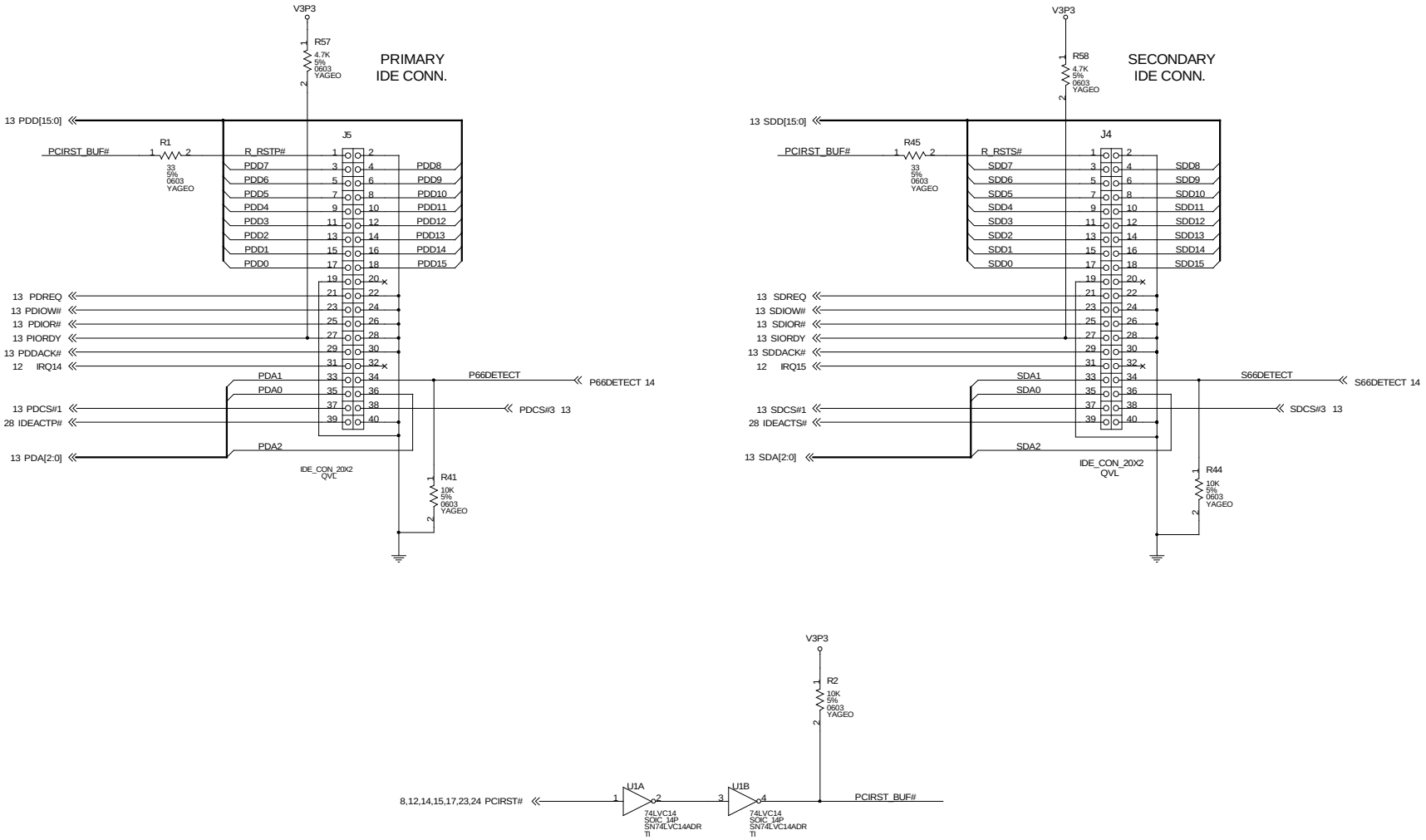


5V PCI CONN., NO 3.3V AND -12V SUPPORT
IDSEL=AD31

THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title	5V PCI R/A CONN.	
Size: C	Document Number: 815E Value Communications Appliance	Rev: A1
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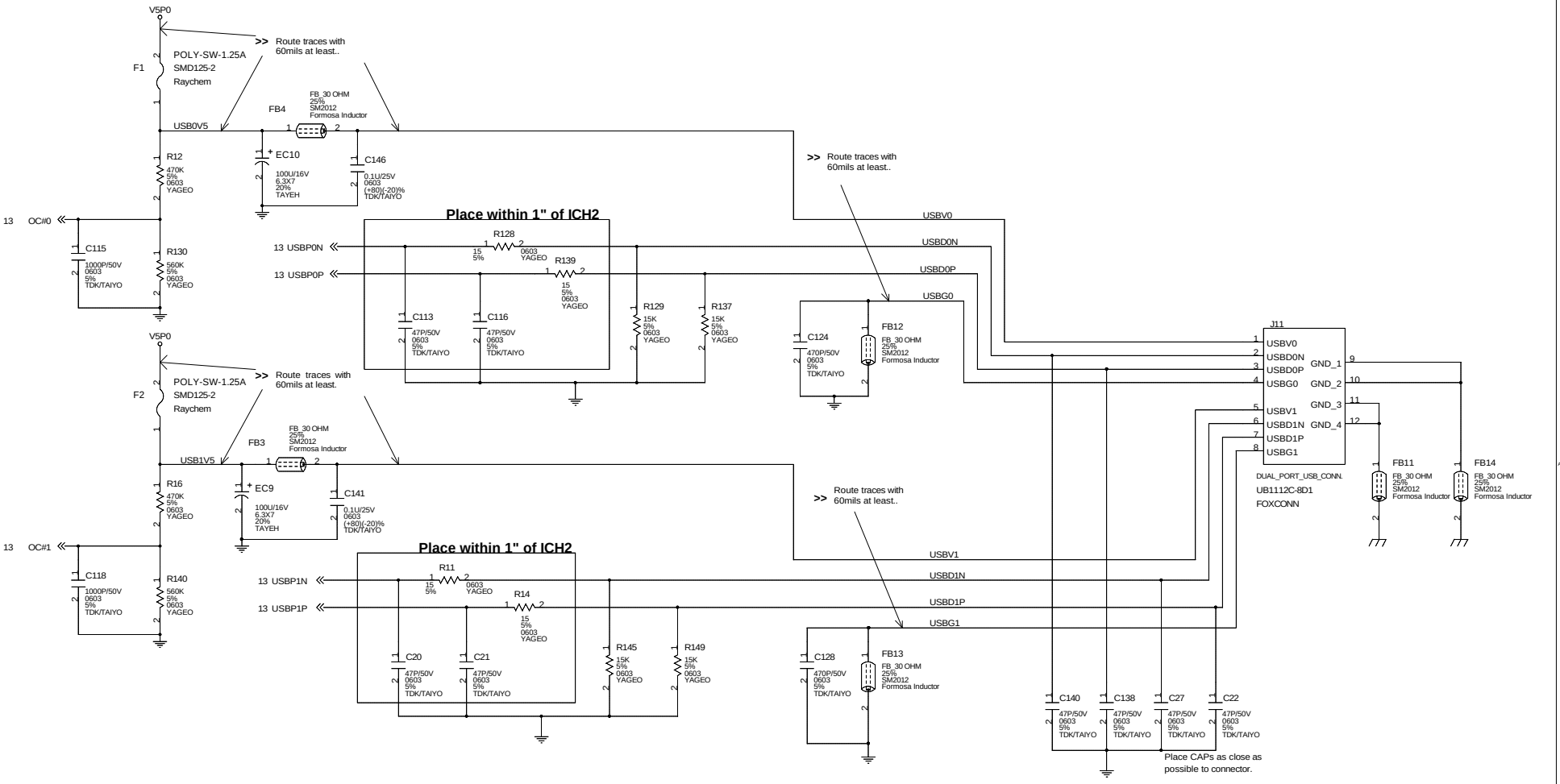
ATA33/66 IDE CONNECTORS



THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title	ATA33/66 IDE CONNECTOR	
Size: C	Document Number: 815E Value Communications Appliance	Rev: A1
Date: Monday, April 09, 2001	Sheet 18 of 34	

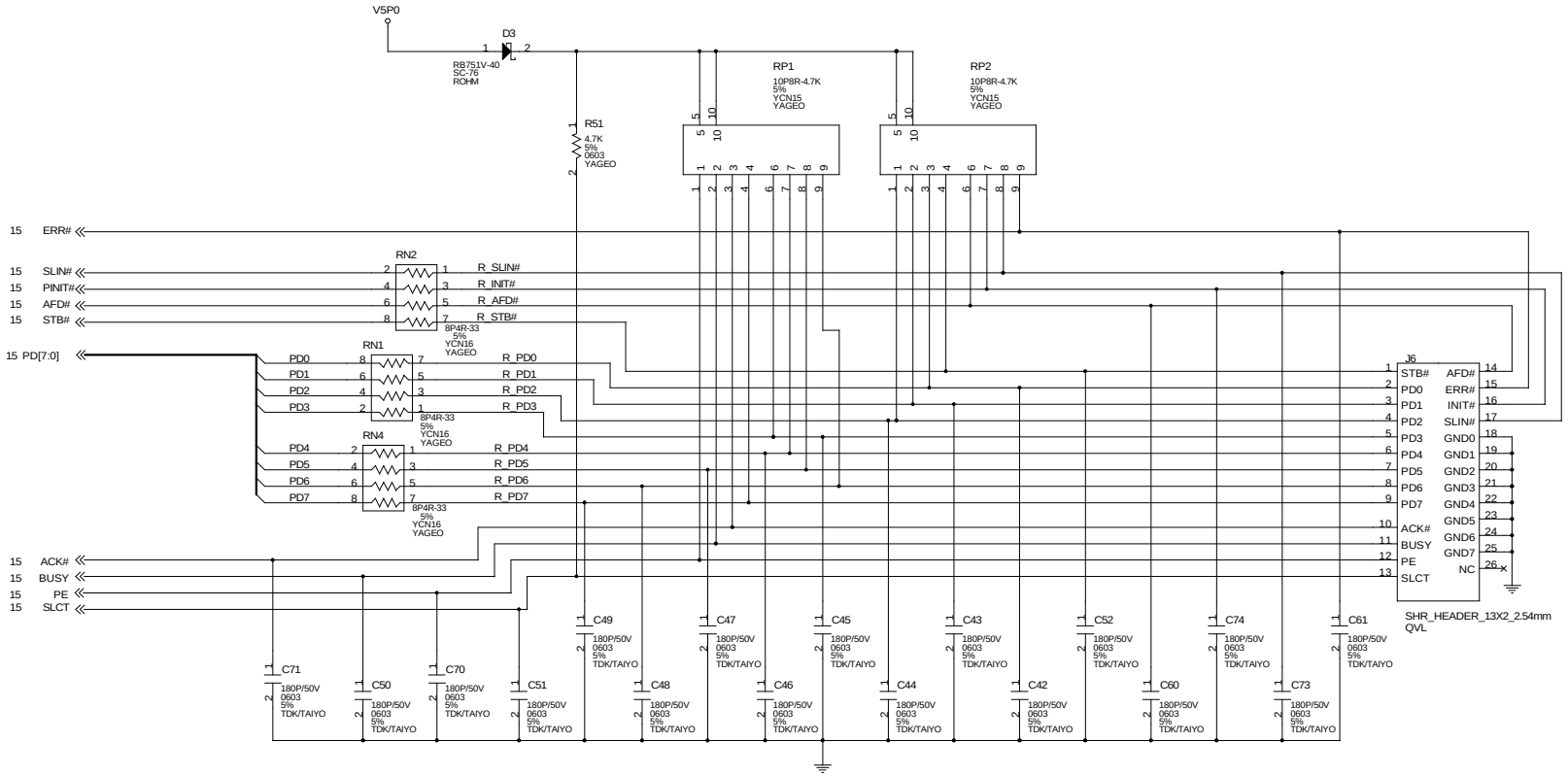
USB Connectors



THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title	USB Connector	
Size: C	Document Number: 815E Value Communications Appliance	Rev: A1
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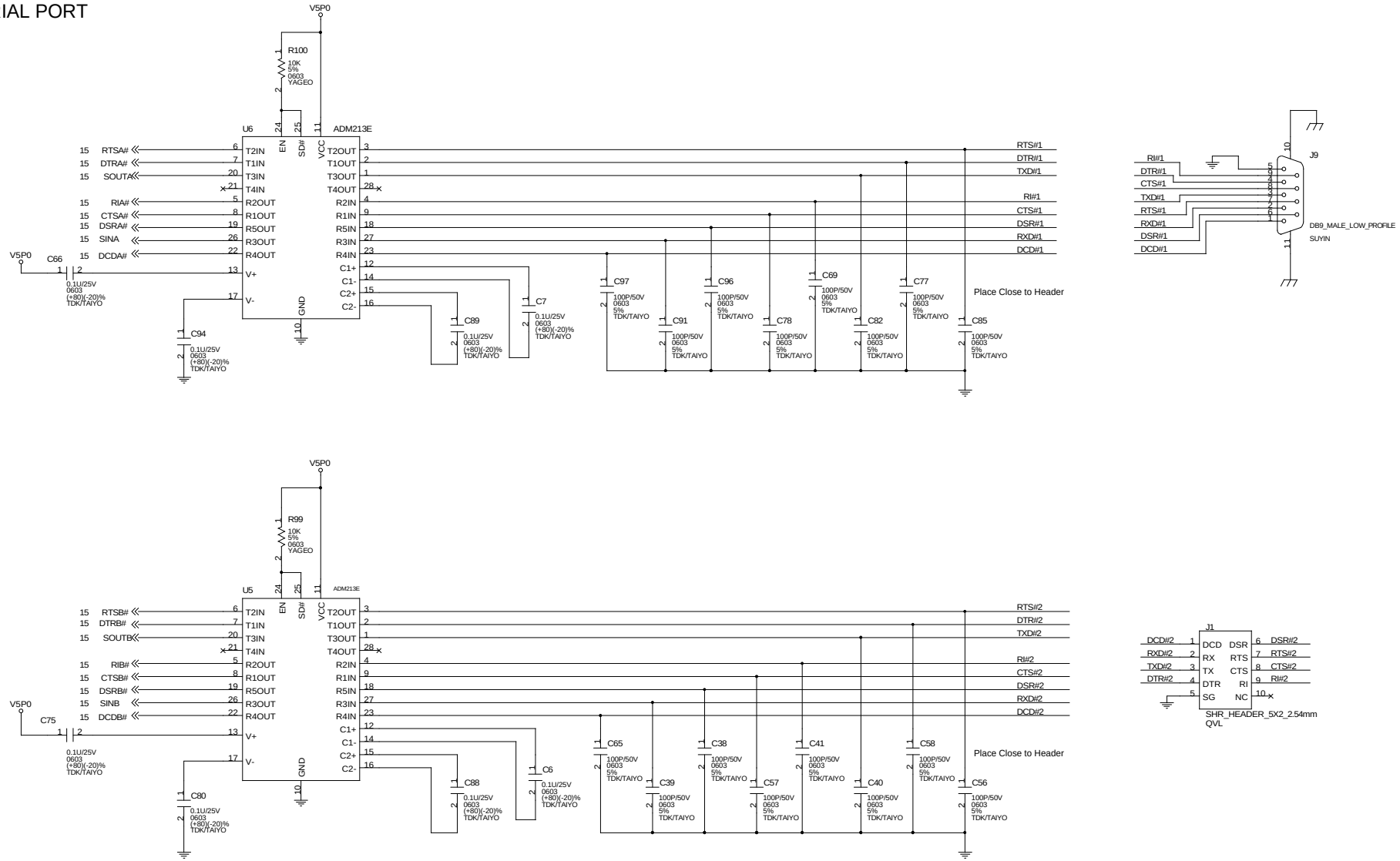
Parallel Port Header



THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title	Parallel Port Header	
Size: C	Document Number: 815E Value Communications Appliance	Rev: A1
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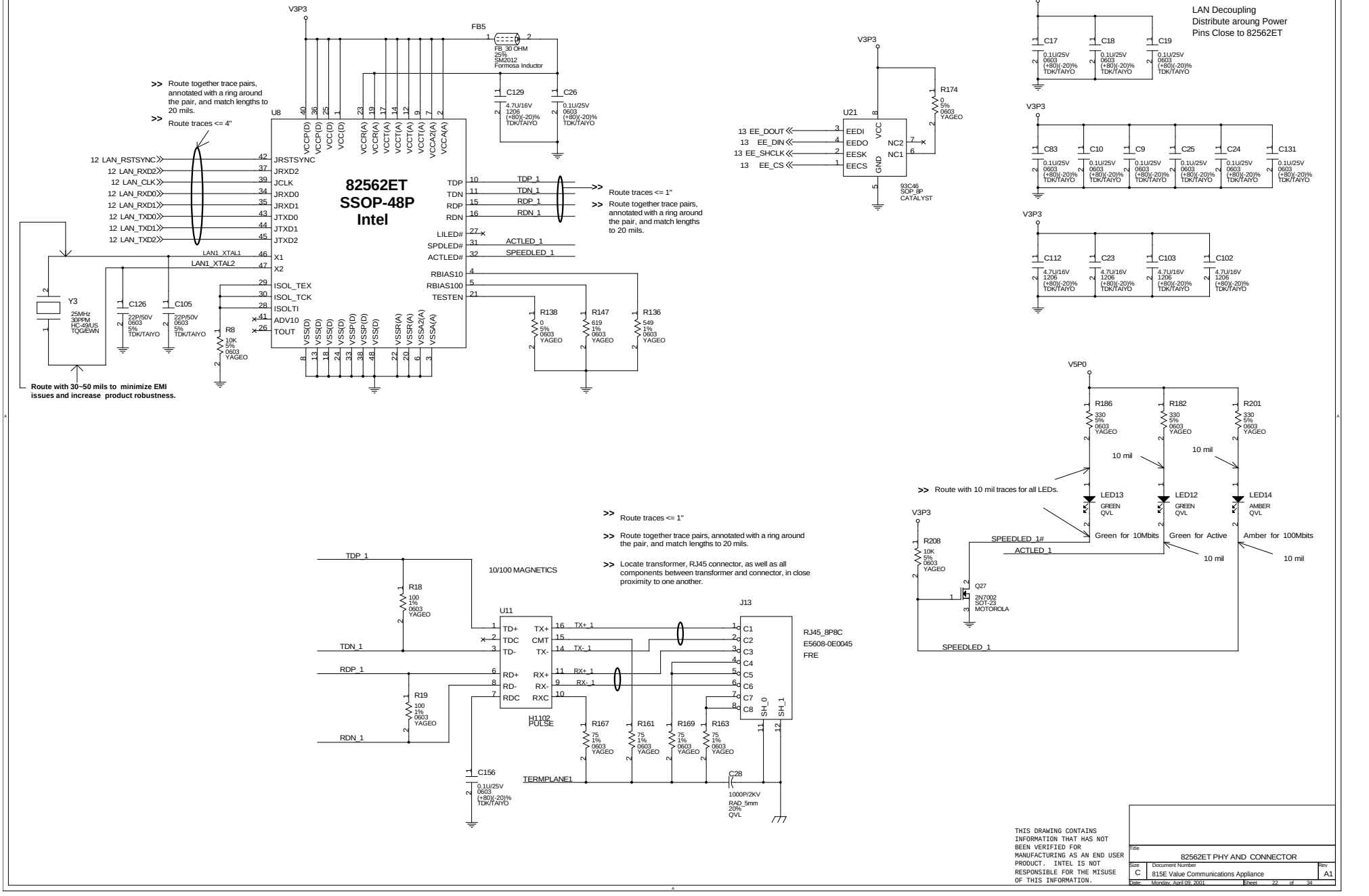
SERIAL PORT



THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

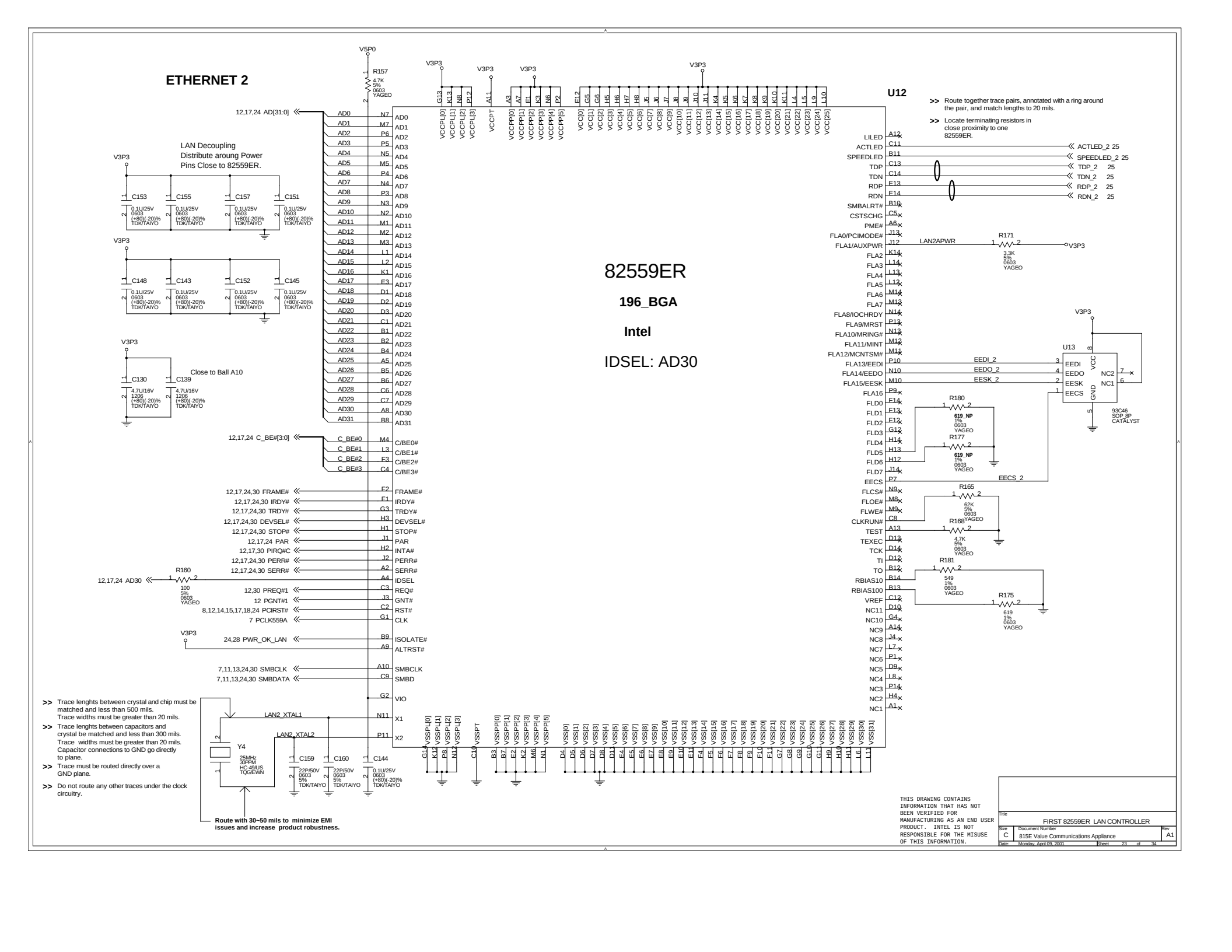
Title	SERIAL PORTS CONN.	
Size: C	Document Number: 815E Value Communications Appliance	Rev: A1
Date: Monday, April 09, 2001	Sheet 21 of 34	

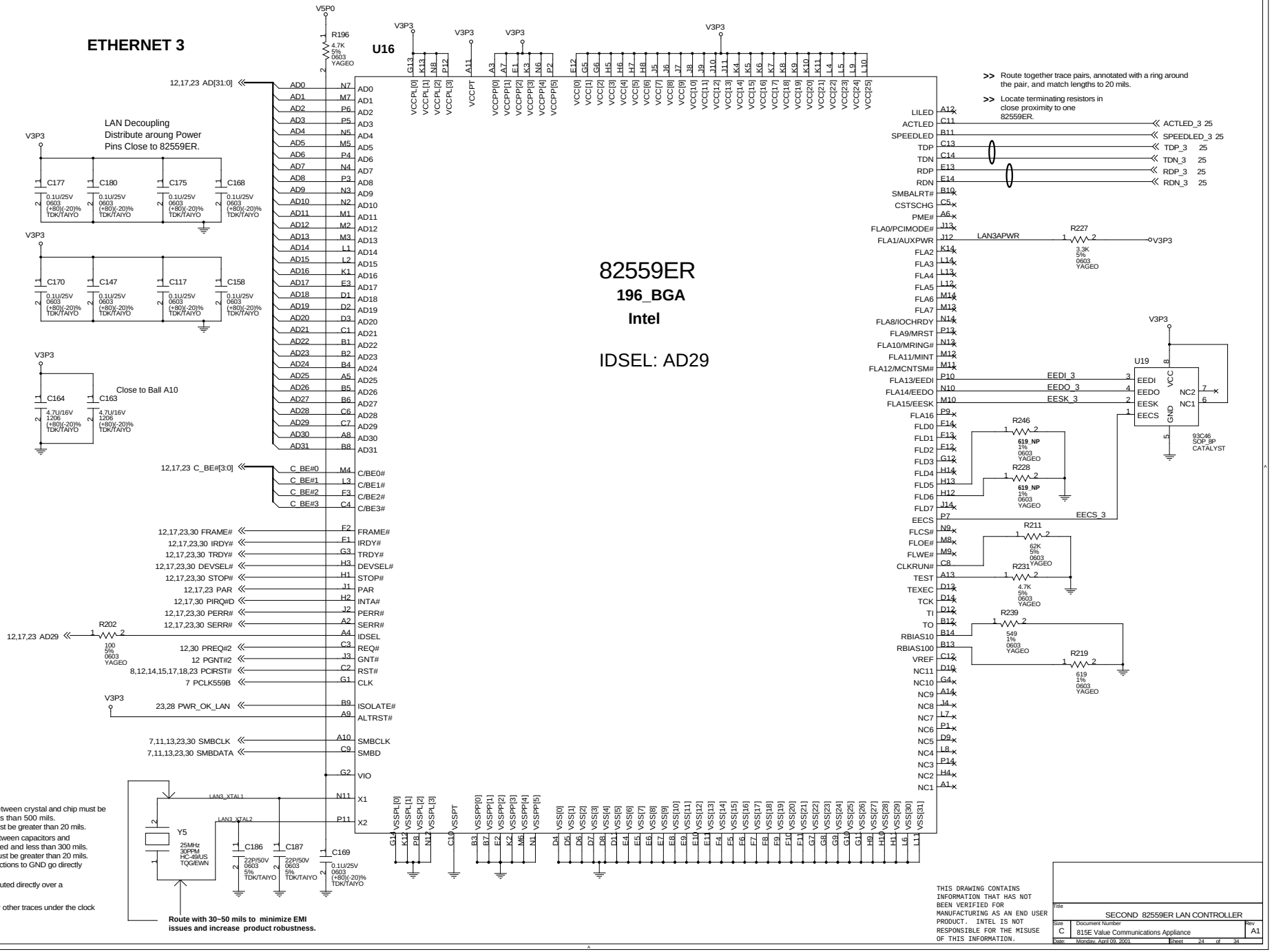
ETHERNET 1



THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

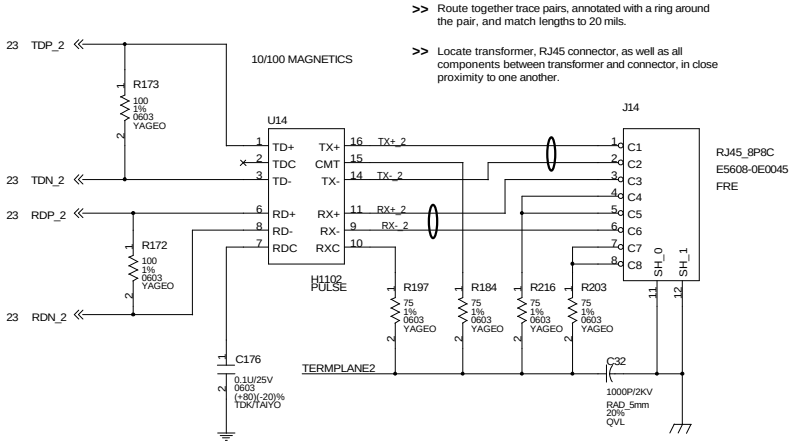
Title	82562ET PHY AND CONNECTOR	
Size: C	Document Number: 815E Value Communications Appliance	Rev: A1
Date: Monday, April 09, 2001	Sheet 22 of 34	

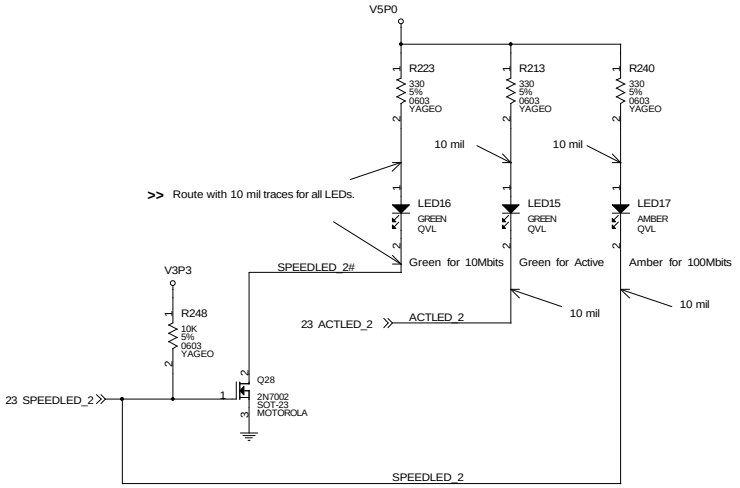

ETHERNET 2
82559ER
196_BGA
Intel
IDSEL: AD30
U12
LAN Decoupling
Distribute aroung Power
Pins Close to 82559ER.
Close to Ball A10
>> Route together trace pairs, annotated with a ring around the pair, and match lengths to 20 mils.
>> Locate terminating resistors in close proximity to one 82559ER.
>> Trace lenghts between crystal and chip must be matched and less than 500 mils. Trace widths must be greater than 20 mils.
>> Trace lenghts between capacitors and crystal be matched and less than 300 mils. Trace widths must be greater than 20 mils. Capacitor connections to GND go directly to plane.
>> Trace must be routed directly over a GND plane.
>> Do not route any other traces under the clock circuitry.
Route with 30~50 mils to minimize EMI issues and increase product robustness.
THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.
FIRST 82559ER LAN CONTROLLER
815E Value Communications Appliance
Monday, April 09, 2001
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ETHERNET 3
U16
82559ER
196_BGA
Intel
IDSEL: AD29
LAN Decoupling
Distribute aroung Power
Pins Close to 82559ER.
Close to Ball A10
>> Route together trace pairs, annotated with a ring around the pair, and match lengths to 20 mils.
>> Locate terminating resistors in close proximity to one 82559ER.
>> Trace lenghts between crystal and chip must be matched and less than 500 mils. Trace widths must be greater than 20 mils.
>> Trace lenghts between capacitors and crystal be matched and less than 300 mils. Trace widths must be greater than 20 mils. Capacitor connections to GND go directly to plane.
>> Trace must be routed directly over a GND plane.
>> Do not route any other traces under the clock circuitry.
Route with 30~50 mils to minimize EMI issues and increase product robustness.
THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.
SECOND 82559ER LAN CONTROLLER
815E Value Communications Appliance
Monday, April 09, 2001
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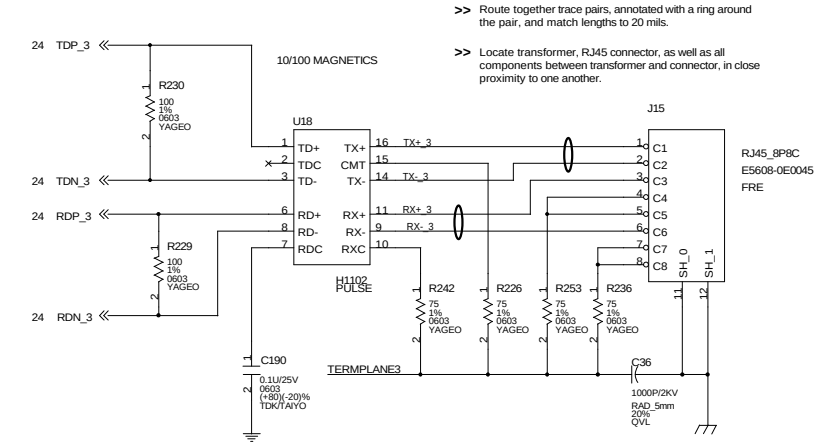
RJ45 CONNECTORS

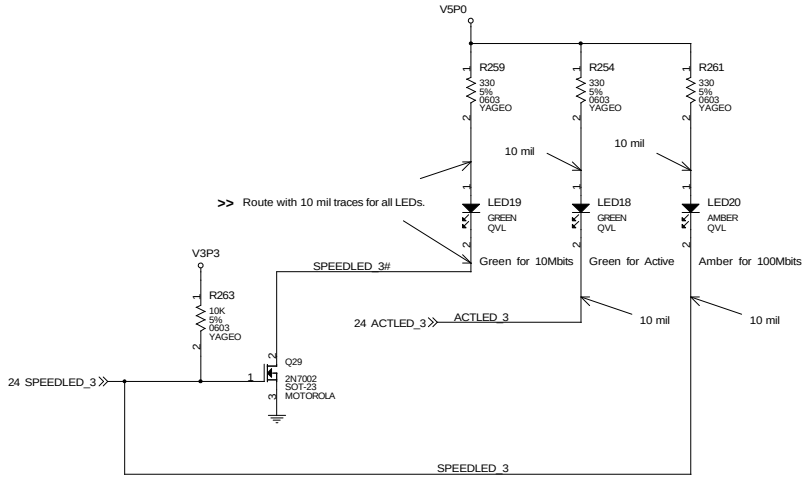
ETHERNET 2





ETHERNET 3

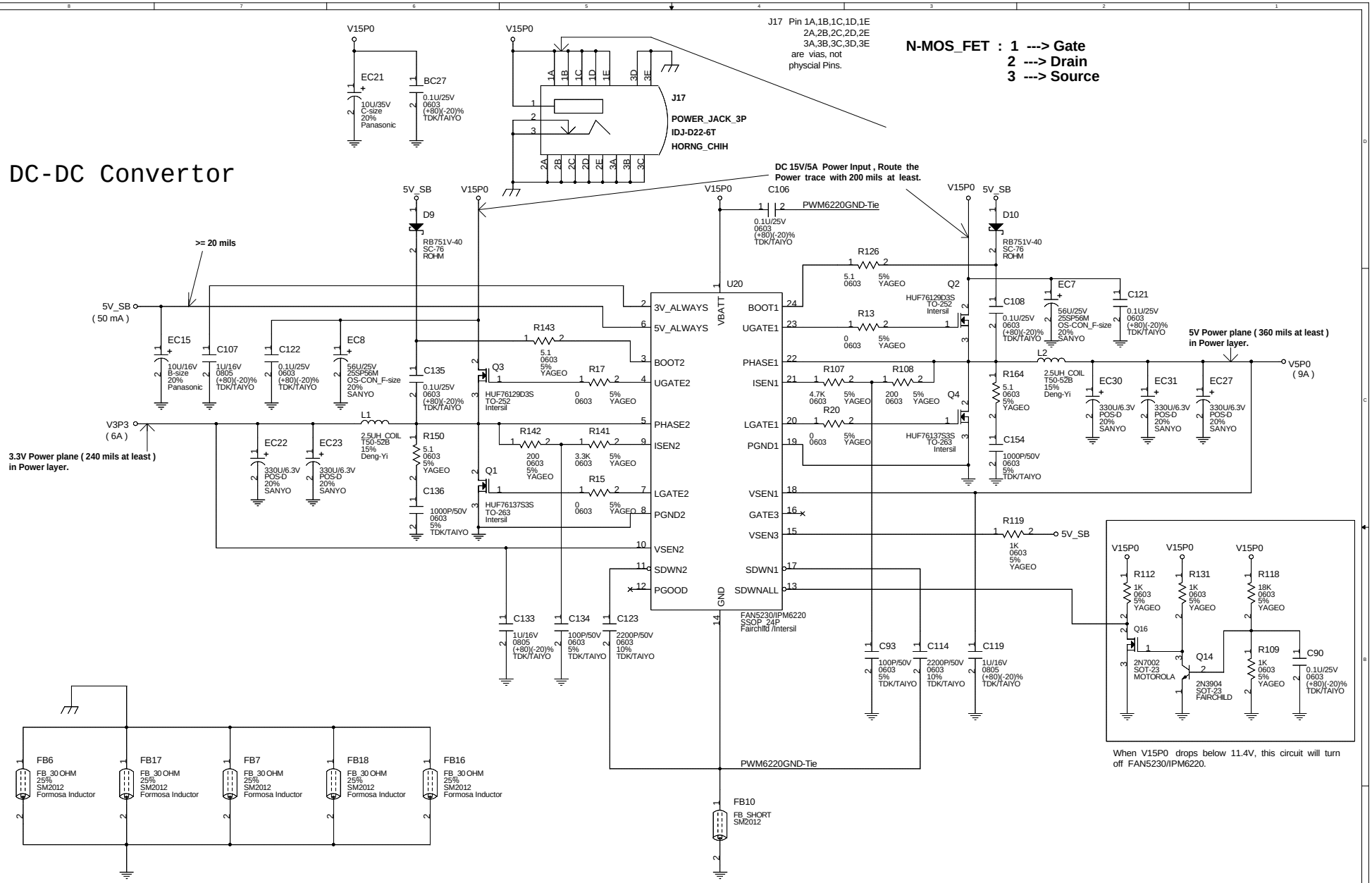




THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title	ETHERNET 2&3 CONNECTOR	
Size: C	Document Number: 815E Value Communications Appliance	Rev: A1
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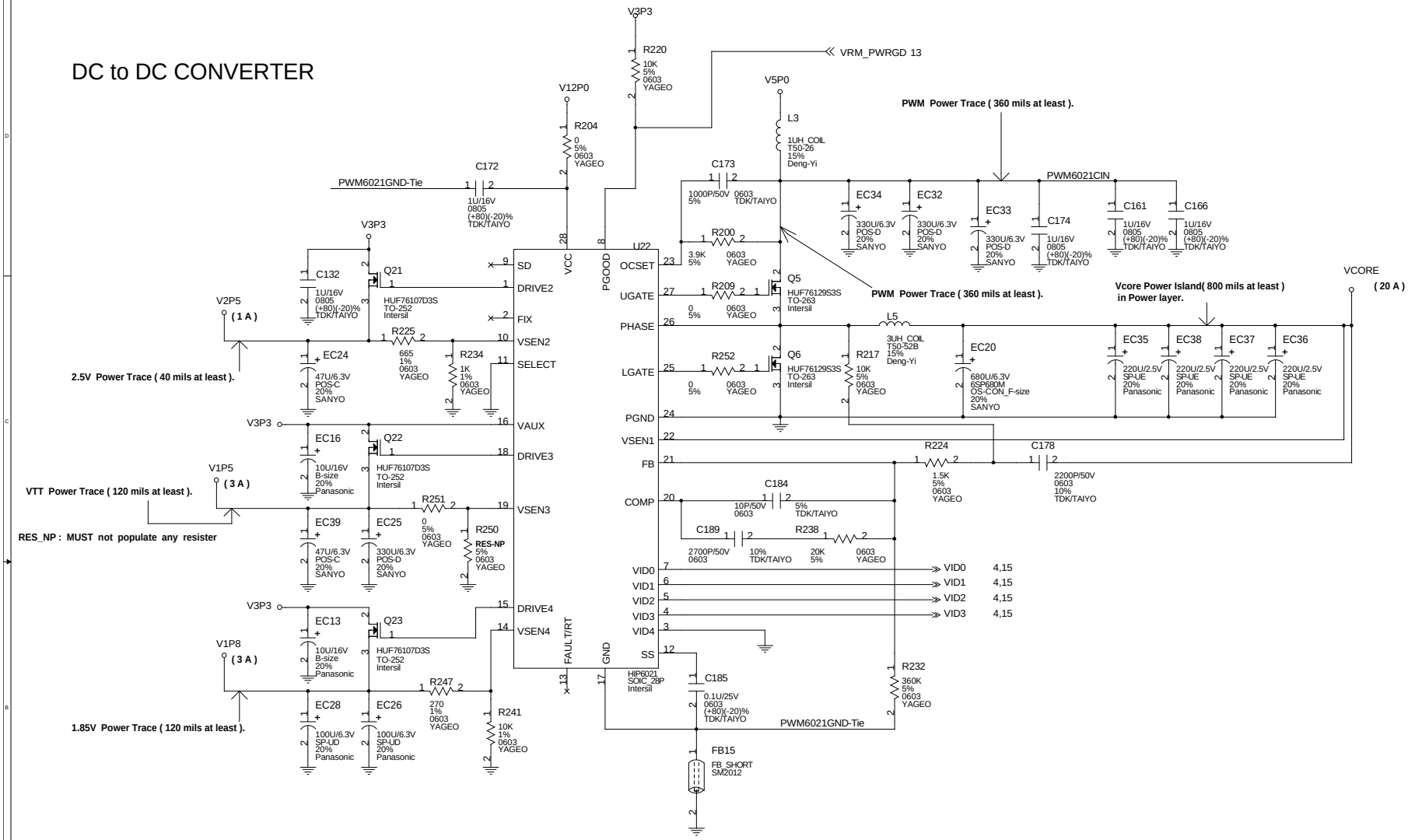
DC-DC Convertor



THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title	DC-TO-DC CONVERTOR AND VRM8.4	
Size: C	Document Number: 815E Value Communications Appliance	Rev: A1
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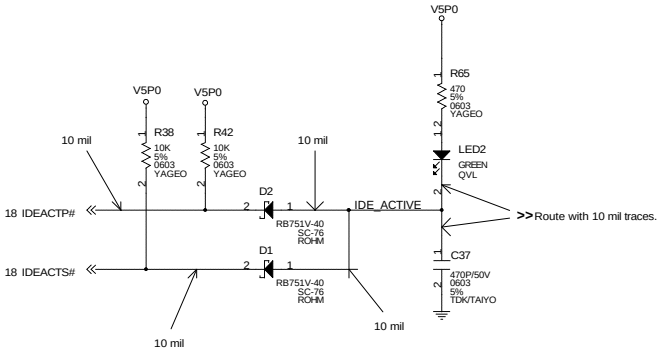
DC to DC CONVERTER



THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

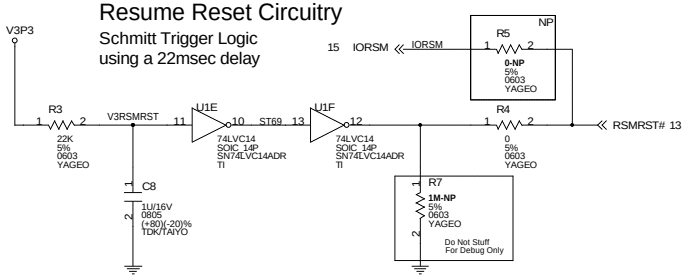
Title	DC-TO-DC CONVERTOR AND VRM8.4	
Size: C	Document Number: 815E Value Communications Appliance	Rev: A1
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Power Connector and Reset Control

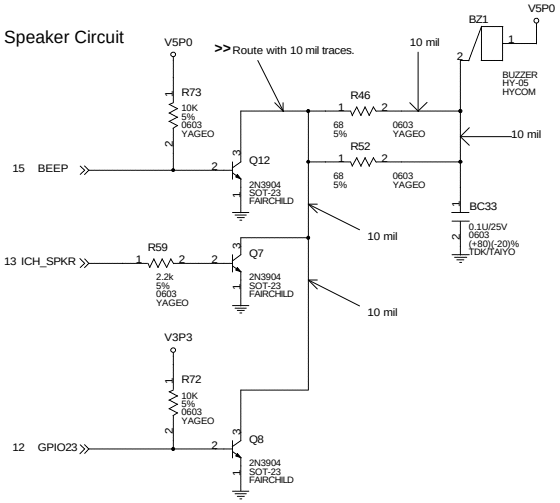


Resume Reset Circuitry

Schmitt Trigger Logic
using a 22msec delay

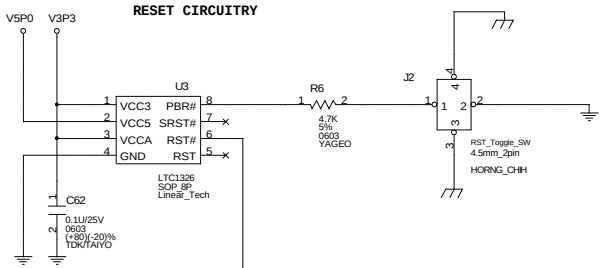


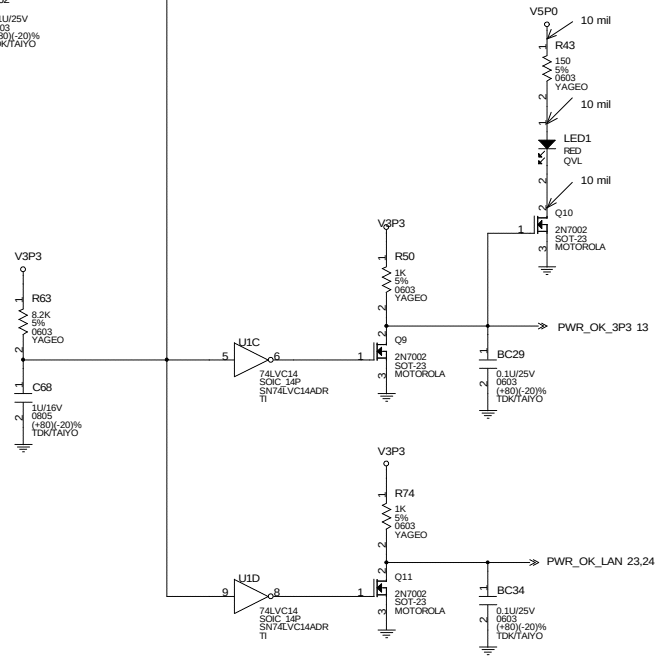
Speaker Circuit

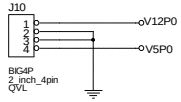


H/W Reset

RESET CIRCUITRY





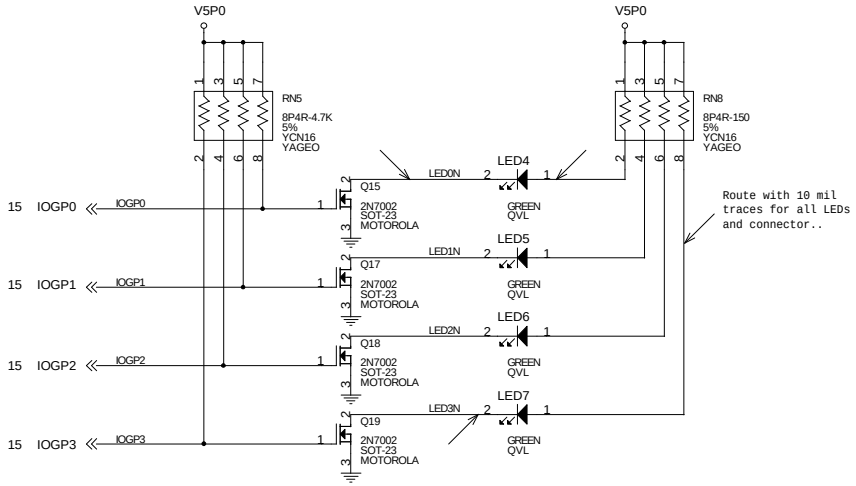


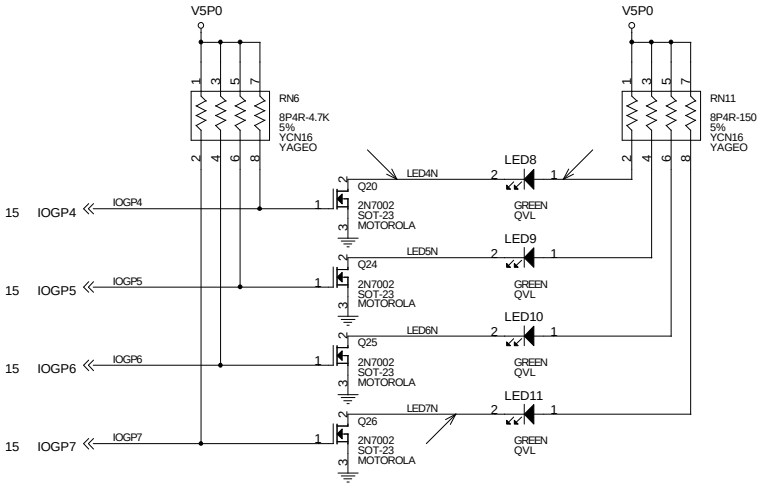
FOR HDD POWER

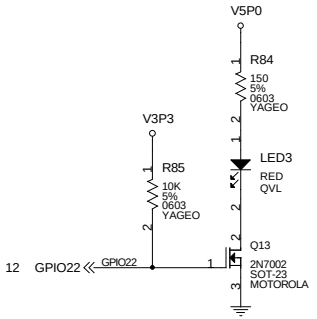
THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title	System Power Connector And Reset Control	
Size: C	Document Number: 815E Value Communications Appliance	Rev: A1
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GPIO LEDs







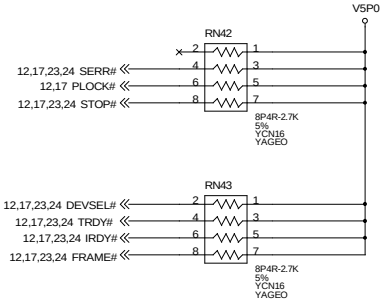
Alert LED

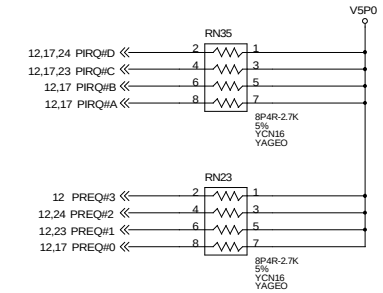
THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

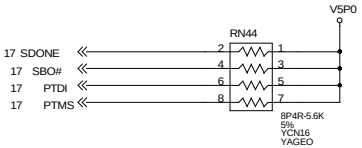
Title	GPIO LED
Size	C
Document Number	815E Value Communications Appliance
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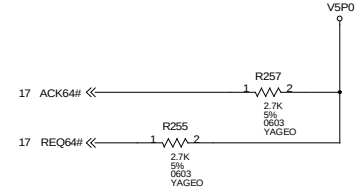
PULL-UP RESISTORS

PCI BUS

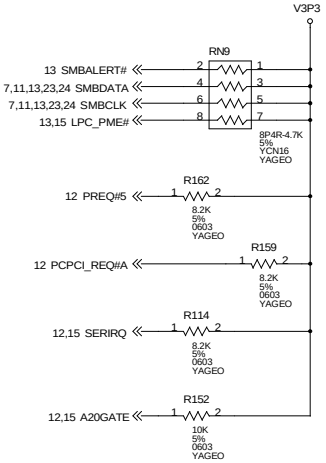


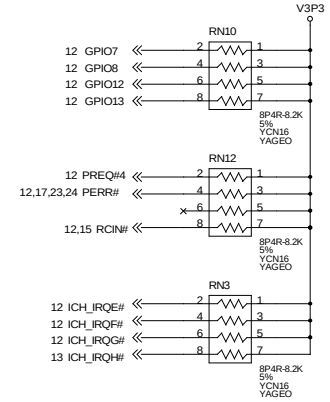




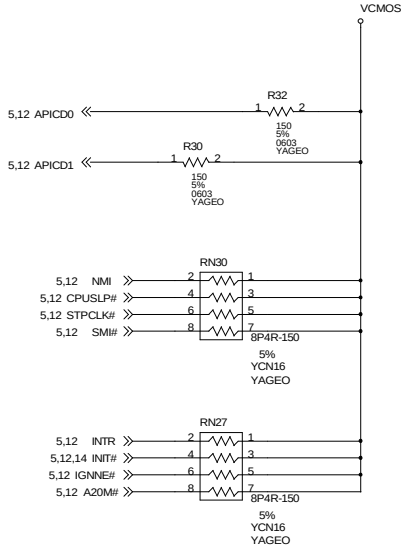


ICH2





CPU



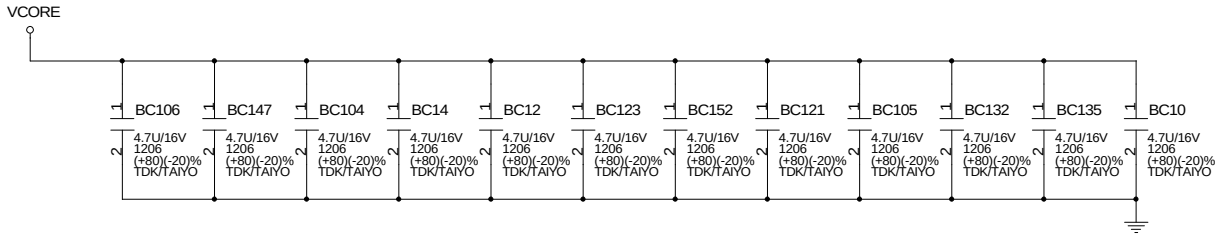
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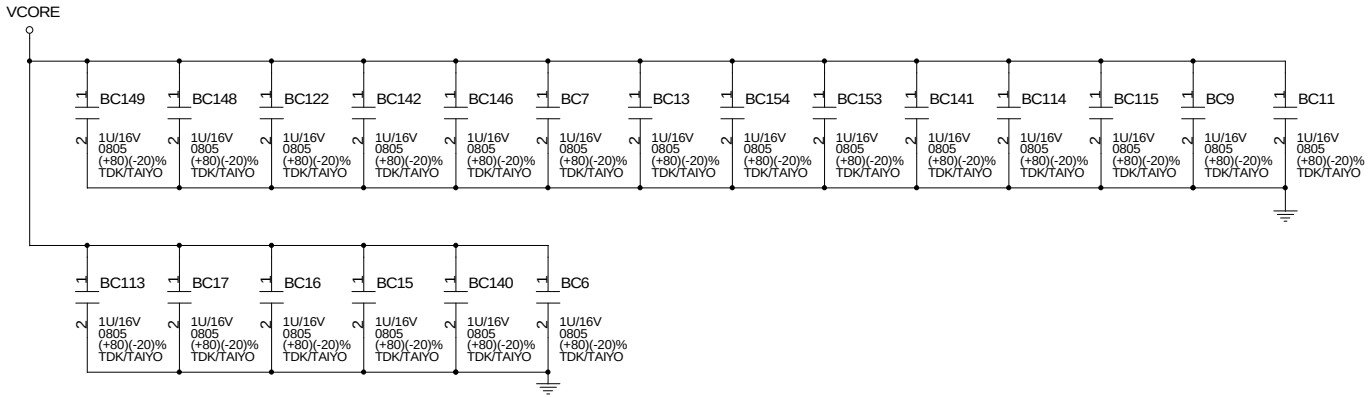
Title	PULL-UP RESISTORS	
Size: C	Document Number: 815E Value Communications Appliance	Rev: A1
Date: Monday, April 09, 2001	Sheet 30 of 34	

PGA370 Decoupling

VCORE Decoupling

Place in PGA370 Socket Cavity





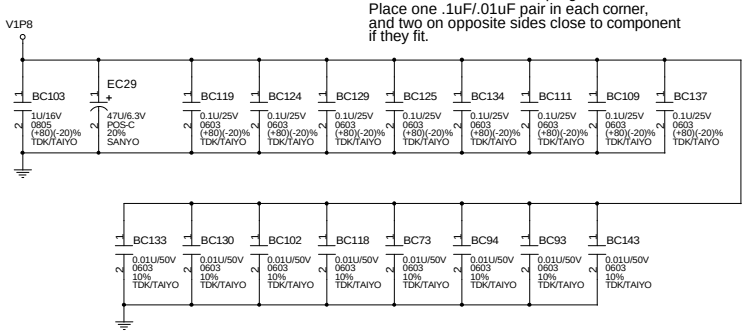
THIS DRAWING CONTAINS INFORMATION THAT HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title	SOCKET 370 DECOUPLING	
Size: B	Document Number: 815E Value Communications Appliance	Rev: A1
Date: Monday, April 09, 2001	Sheet 31 of 34	

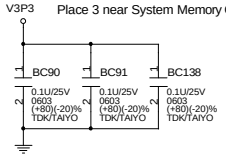
DRAM, CHIPSET, and BULK POWER DECOUPLING

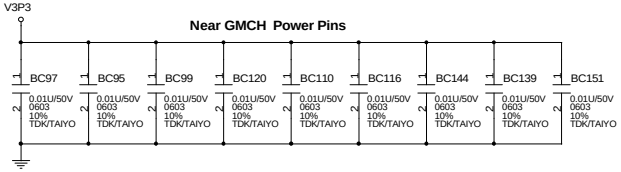
GMCH Decoupling

GMCH Core Plane Decoupling:
Place one .1uF/.01uF pair in each corner,
and two on opposite sides close to component
if they fit.



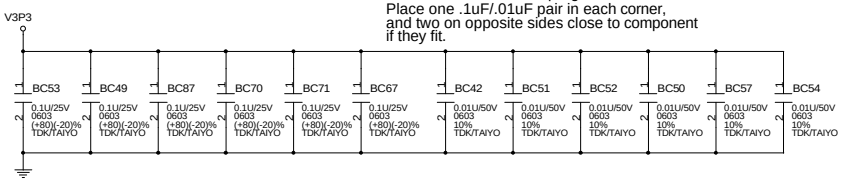
GMCH 3.3V IO Decoupling:
Place 3 near System Memory Quadrant



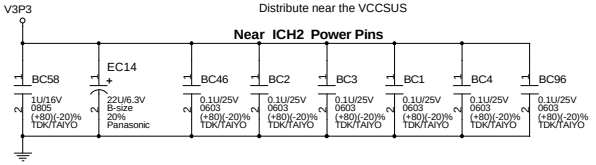


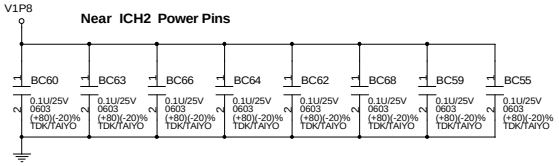
ICH2 Decoupling

ICH2 3.3V Plane Decoupling:
Place one .1uF/.01uF pair in each corner,
and two on opposite sides close to component
if they fit.



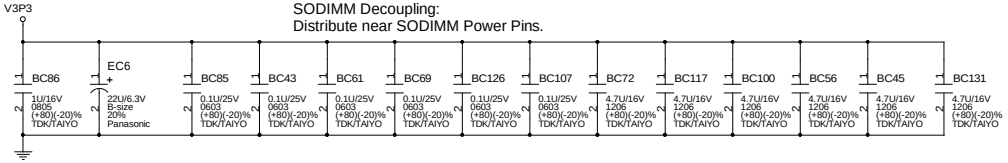
Distribute near the VCCSUS
Near ICH2 Power Pins



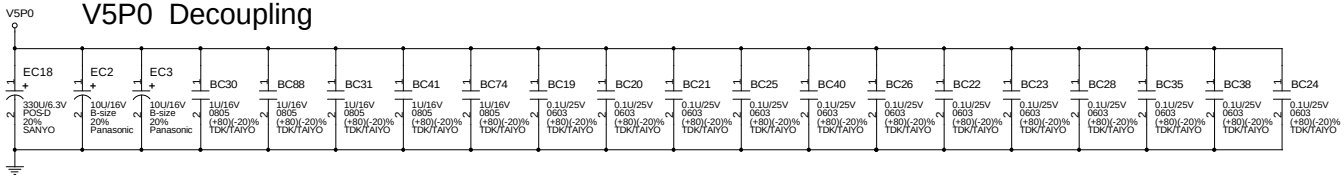


System Memory Decoupling

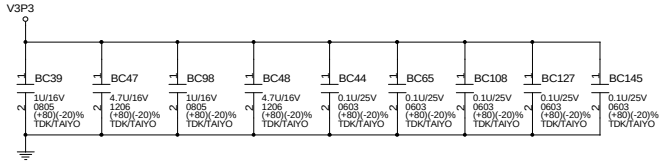
SODIMM Decoupling:
Distribute near SODIMM Power Pins.

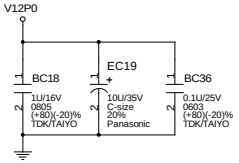


V5P0 Decoupling



Misc. Power Decoupling





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Title: CHIPSET AND BULK DECOUPLING
Size: C | Document Number: 815E Value Communications Appliance | Rev: A1
Date: Monday, April 09, 2001 | Sheet 32 of 34

CONNECTOR TABLES

LED-GPIO TABLE

LED Ref.	LED Color	Which GPIO control?	Function	S/W Programmable?	Default status by BIOS programming
LED1	RED	N/A	Power Okay indicator ON: Okay, OFF: Bad.	NO	N/A
LED2	GREEN	N/A	HDD Active Indicator ON: HDD activated, OFF: HDD non-activated	NO	N/A
LED3	RED	ICH2-GPIO22	Alert LED ON : Abnormal OFF : Normal	YES	Turn OFF
LED4	GREEN	83627HF-GP10	GP_LED0	YES	Turn ON
LED5	GREEN	83627HF-GP11	GP_LED1	YES	Turn ON
LED6	GREEN	83627HF-GP12	GP_LED2	YES	Turn ON
LED7	GREEN	83627HF-GP13	GP_LED3	YES	Turn ON
LED8	GREEN	83627HF-GP14	GP_LED4	YES	Turn ON
LED9	GREEN	83627HF-GP15	GP_LED5	YES	Turn ON
LED10	GREEN	83627HF-GP16	GP_LED6	YES	Turn ON
LED11	GREEN	83627HF-GP17	GP_LED7	YES	Turn ON
LED12	GREEN	N/A	LAN1_ACTIVE LED ON : LAN1 Active OFF : Non Active	NO	N/A
LED13	GREEN	N/A	LAN1_LINK 10Mb ON : Link to 10Mb OFF : No link to 10Mb	NO	N/A
LED14	AMBER	N/A	LAN1_LINK 100Mb ON : Link to 100Mb OFF : No link to 100Mb	NO	N/A
LED15	GREEN	N/A	LAN2_ACTIVE LED ON : LAN2 Active OFF : Non Active	NO	N/A
LED16	GREEN	N/A	LAN2_LINK 10Mb ON : Link to 10Mb OFF : No link to 10Mb	NO	N/A
LED17	AMBER	N/A	LAN2_LINK 100Mb ON : Link to 100Mb OFF : No link to 100Mb	NO	N/A
LED18	GREEN	N/A	LAN3_ACTIVE LED ON : LAN3 Active OFF : Non Active	NO	N/A
LED19	GREEN	N/A	LAN3_LINK 10Mb ON : Link to 10Mb OFF : No link to 10Mb	NO	N/A
LED20	AMBER	N/A	LAN3_LINK 100Mb ON : Link to 100Mb OFF : No link to 100Mb	NO	N/A

JUMPER TABLE

JUMPER Ref.	FUNCTION	DEFAULT¡@SETTING
JP1	CLEAR CMOS RAM 1-2 : Normal 2-3 : CLEAR CMOS RAM	1-2 : Normal
JP2	CPU Frequency Strapping IN : Force CPU Frequency to safe mode OUT : Use CPU Frequency strapping in ICH2 Register	OUT : By ICH2 Reg.
JP3	FWH Top Block LOCK IN : TOP BLOCK UNLOCK OUT : TOP BLOCK LOCK	IN : UNLOCK

J1/J9 Serial Port connector(Page 21)
J1 : 2x5 Pin Header, J9 : D-SUB9 Male

Pin Number	Signal Description
1	DCD
2	RXD
3	TXD
4	DTR
5	SGND
6	DSR
7	RTS
8	CTS
9	RI
10	N/C (J1 Only)

J2 : Reset push button (Momentary),Page 28

Pin Number	Signal Description
1	Reset signal
2	Ground

J3 : FDC(17x2) Connector , Page 15

P.N.	Description	P.N.	Description
1	Ground	2	Density0#
3	Ground	4	N/C
5	Ground	6	Density1#
7	Ground	8	INDEX#
9	Ground	10	MOA#
11	Ground	12	DSB#
13	Ground	14	DSA#
15	Ground	16	MOB#
17	Ground	18	DIR#
19	Ground	20	STEP#
21	Ground	22	WD#
23	Ground	24	WE#
25	Ground	26	TRACK0#
27	Ground	28	WP#
29	N/C	30	RDATA#
31	Ground	32	HEAD#
33	N/C	34	DSKCHG#

J4/J5 : IDE(20x2) Connector,Page 18

P.N.	Description	P.N.	Description
1	RESET#	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	N/C
21	DMAREQ	22	Ground
23	IOW#	24	Ground
25	IOR#	26	Ground
27	IOCHRDY	28	Ground
29	DMAACK#	30	Ground
31	IRQ15/14	32	N/C
33	SA1	34	PDIAG#/CSEL
35	SA0	36	SA2
37	HDCCS0#	38	HDCCS1#
39	HDDACTIVE#	40	Ground

J6 : Parallel Port (13x2) Connector, Page 20

P.N.	Description	P.N.	Description
1	Strobe#	14	AFD#
2	Data 0	15	ERR#
3	Data 1	16	INIT#
4	Data 2	17	SLIN#
5	Data 3	18	Ground
6	Data 4	19	Ground
7	Data 5	20	Ground
8	Data 6	21	Ground
9	Data 7	22	Ground
10	ACK#	23	Ground
11	BUSY	24	Ground
12	PE	25	Ground
13	SLCT	26	N/C

J7/J8/J16 :TachoMeter FAN Connector, Page 16
J7, J8 for chassis Fan
J16 for CPU Fan

Pin Number	Signal Description
1	Ground
2	V12P0
3	TachoMeter Signal

J10 : Power output connector to HDD, Page 28

Pin Number	Signal Description
1	V12P0
2	Ground
3	Ground
4	V5P0

J11 : Dual USB Port Connector, Page 19

P.N.	Description	P.N.	Description
1	5VP0	5	5VP0
2	USBD0-	6	USBD1-
3	USBD0+	7	USBD1+
4	Ground	8	Ground

J12 : VGA Board(6x2) Connector, Page 10

P.N.	Description	P.N.	Description
1	VID_RED	2	Ground
3	VID_GREEN	4	V1P8
5	VID_BLUE	6	Ground
7	Ground	8	3VDDCDA
9	3VDDCCL	10	CRT_HSYNC
11	CRT_VSYNC	12	V5P0

J13/J14/J15 : Ethernet RJ45(8P8C) Connector, Page 22,25
J13: Page 22
J14,J15 : Page 25

P.N.	Description	P.N.	Description
1	TX+	2	TX-
3	RX+	4	Termplane
5	Termplane	6	RX-
7	Termplane	8	Termplane

J17 : DC15V/5A Power Jack Connector, Page 26

Pin Number	Signal Description
1	V15P0
2	Ground
3	Ground

J18 : PCI BUS CONNECTOR ,Page 17

P.N.	Description	P.N.	Description
B1	N/C	A1	PTRST#
B2	PTCK	A2	V12P0
B3	Ground	A3	PTMS
B4	N/C	A4	PTDI
B5	V5P0	A5	V5P0
B6	V5P0	A6	PIRQ#B
B7	PIRQ#C	A7	PIRQ#D
B8	PIRQ#A	A8	V5P0
B9	N/C	A9	N/C
B10	N/C	A10	V5P0
B11	N/C	A11	N/C
B12	Ground	A12	Ground
B13	Ground	A13	Ground
B14	N/C	A14	N/C
B15	Ground	A15	PCIRST#
B16	PCICLK	A16	V5P0
B17	Ground	A17	PGNT#0
B18	PREQ#0	A18	Ground
B19	V5P0	A19	N/C
B20	AD31	A20	AD30
B21	AD29	A21	N/C
B22	Ground	A22	AD28
B23	AD27	A23	AD26
B24	AD25	A24	Ground
B25	N/C	A25	AD24
B26	C_BE#3	A26	IDSEL
B27	AD23	A27	N/C
B28	Ground	A28	AD22
B29	AD21	A29	AD20
B30	AD19	A30	Ground
B31	N/C	A31	AD18
B32	AD17	A32	AD16
B33	C_BE#2	A33	N/C
B34	Ground	A34	FRAME#
B35	IRDY#	A35	Ground
B36	N/C	A36	TRDY#
B37	DEVSEL#	A37	Ground
B38	Ground	A38	STOP#
B39	PLOCK#	A39	N/C
B40	PERR#	A40	SDONE
B41	N/C	A41	SBO#
B42	SERR#	A42	Ground
B43	N/C	A43	PAR
B44	C_BE#1	A44	AD15
B45	AD14	A45	N/C
B46	Ground	A46	AD13
B47	AD12	A47	AD11
B48	AD10	A48	Ground
B49	Ground	A49	AD9
	KEY		KEY
	KEY		KEY
B52	AD8	A52	C_BE#0
B53	AD7	A53	N/C
B54	N/C	A54	AD6
B55	AD5	A55	AD4
B56	AD3	A56	Ground
B57	Ground	A57	AD2
B58	AD1	A58	AD0
B59	V5P0	A59	V5P0
B60	ACK64#	A60	REQ64#
B61	V5P0	A61	V5P0
B62	V5P0	A62	V5P0

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